

RCS file: /s6/cvsroot/euterpe/BOM,v

Working file: BOM

head: 5.105

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 1940; selected revisions: 22

description:

top level BOM

revision 3.588

date: 1995/04/13 23:49:50; author: woody; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

uu:

Update placement to latest version. Still bigger than geert wants. Using some of the 4 rows above the reg file.

uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the 4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWedX1 timing fix.

au: auindx: timmg fix.

cp:

disable an internal mapping of cerberus space to flash rom.

this function is only allowed by an external master poking at location '0'

location '0' and '1' boot from local rom.

all others boot over cerberus to master at location '0'

might be others

revision 3.587

date: 1995/04/13 21:14:31; author: geert; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

Makefile.share

Changed number of iterations to 2

Geert

revision 3.586

date: 1995/04/13 21:06:58; author: doi; state: Exp; lines: +2 -2

Release Target: euterpe/verify/ukernel

used the _real_ boot instead of boot_pl_kernel by mistake

revision 3.585

date: 1995/04/13 07:02:16; author: dickson; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/mc

move mc to the rigth 12 rows

revision 3.584

date: 1995/04/13 06:56:13; author: dickson; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/es

remove another 12atoms in width

revision 3.583

date: 1995/04/12 23:15:21; author: dickson; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/ctiod

timing fix

revision 3.582

date: 1995/04/12 20:20:03; author: mws; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

rg/rgpc.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:

Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.

ALL (almost all) TESTS WILL NEED TO BE RECOMPILED.

Placement is not affected.

revision 3.581

date: 1995/04/12 16:17:19; author: billz; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/cc

Since the latest placement, hasn't made it into the latest bsrc/BOM,
(276.2) I'm releasing now.

revision 3.580

date: 1995/04/12 04:08:48; author: woody; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/lt

Added flop in snkReq path. This allows the signal from GT to be half-swing and
should fix the timing problem.

revision 3.579

date: 1995/04/12 03:59:18; author: woody; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/at

Added cdMissR12 to UvldStrR13/*UvldDcachStrR13*/. The dtag dirty bit was being
set by a store that gets a cache Miss. Test synch_1 noticed. Now it will only
write dirty bit if there was a cache hit.

revision 3.578

date: 1995/04/12 03:30:02; author: mws; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

rg/rgpc.V rg/rg.V rgxmit/rgxmit.V uu/uu.V euterpe.V \

rg/rg.pim rgxmit/rgxmit_control.pim:

Eliminate midpipe undo increment feature by moving predicted br inc
suppression controls backward in pipe. Saves muxff2_62 (a strip at
least 7 atoms wide 434 atoms total) and associated metal4.

uu/gen_mem.pl uu/uu_drive.V: Update reserved xlu instr tests to drive X's
in the register number fields when possible.

uu/uumic.tst: Add a predicted taken blinki case.

tst/job.tst: r[abc] and op[abc] &OpPreps done before \$RDst stuff ready.

cdio/cdio.V: Was copying the low datain to high datain for the 2nd half of
the CD write cycle.

revision 3.577
date: 1995/04/12 01:36:10; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/gf

timing fix

revision 3.576
date: 1995/04/11 23:19:16; author: bobm; state: Exp; lines: +2 -2
Release Target: euterpe/doc
euterpe-microarch.book
front.mif
euterpe-microarchTOC.mif
intro.mif
opcodes.mif
xlu.mif
pipeline.mif
memory.mif
events.mif
reset.mif
cerberus.mif
newchanges.mif

Release of version 1.8 of Euterpe MicroArchitecture. There are some changes to this version, but basically I'm releasing it before incorporating review changes.

revision 3.575
date: 1995/04/11 18:58:57; author: woody; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

Fix typo.

revision 3.574
date: 1995/04/11 17:18:55; author: woody; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

Add flop in ltDone path to make it half-swing.

revision 3.573
date: 1995/04/11 07:44:21; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

Noncrashing placements for rg, au (no change), rgxmit, lt, at.
This leaves just uu, ife, and icc yet to place.
Also grab new veena reserved instr tests in uu.

revision 3.572
date: 1995/04/10 22:44:00; author: doi; state: Exp; lines: +2 -2
Release Target: euterpe/verify
Makefile
Makefile.rules
Makefile.defs

Makefile: Changed and added some targets for dummy_boot.
Makefile.rules: Got rid of %.rom rule and moved it into

```

        verify/ukernel/Makefile/
Makefile.defs:    Added definition for mergesections tool.
                  Removed paths to nanoboot, boot, ukernel, etc. and put them
                  into verify/ukernel/Makefile.
-----
revision 3.571
date: 1995/04/10 22:35:51;  author: doi;   state: Exp;   lines: +2 -2
Release Target:  euterpe/verify/tools

new mergesections tool
-----
revision 3.570
date: 1995/04/10 22:31:25;  author: doi;   state: Exp;   lines: +2 -2
Release Target:  euterpe/verify/ukernel

time for a rebuild
-----
revision 3.569
date: 1995/04/10 19:52:41;  author: dickson; state: Exp;   lines: +2 -2
Release Target:  euterpe/verilog/bsrc/es

move es to right more redid some alms and summation instruction changes
-----
revision 3.568
date: 1995/04/10 19:47:22;  author: dickson; state: Exp;   lines: +2 -2
Release Target:  euterpe/verilog/bsrc/mc

move mc to the right
-----
revision 3.567
date: 1995/04/09 10:42:04;  author: mws;   state: Exp;   lines: +2 -2
Release Target:  euterpe/verilog/bsrc

HEAD FOR THE HILLS -- This is a huge change.  Placements coming later.
Main pipe PC was updated too late on branches to be used on trgt ITag mtch.
    Tests tlb_1 and probably any unix notice.
Main pipe PL was updated too late on branches to be used on trgt ITag mtch.
    Even worse, it was way too late for LTLB to check br adrs on behalf of trgt.
    Found by inspection, maybe icache_except might notice.
rg/rgpc.V rg/rg.V euterpe.V:
    Delete pcr3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
    Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
icc/icc.V icc/icc.control.pim euterpe.V:
    Add 5 stage shift register & snapper so ICC can capture a gva[63:48] on
    branches and thus no longer need to continous ltlb of its own and so it
    can get high gva in time for use on target.
icc/icc.V icc/icc.control.pim: Pipe for plR4 was 1 stage too short causing
    cylinders to use others' priv levels.  Probably is mostly responsible for
    test icache_except failure, but see bsrc/euterpe.status for another PL bug.
ife/ife.V ife/ifpcselil.Veqn: Merge ifp sel & ciRdNdx muxes in I2 stage
    by getting rid of tag index mux fanin on ciRdNdx.
ife/ife.V ife/ifpcselil.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe
    and snapped miss gva [47:12] to ICC so all in uniform place and to cut
    control back & forth.
ife/ife.V: Detect mispredict recovery to sequential new

```

```

page & request corresponding hiccup to check protection. Found by inspection;
sinister protection implications if were not found.
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg??pim:
Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
Delete pc[63:48] sent to for ICC's version of ltlb translation.
Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.
at/atpaselgen8.Veqn (delete) at/atpaselgen8.V (add) at/Makefile:
Reimplement so that gva input can be halfswing to handle new run to ICC.
at/at.V: Reorder dor pins into UfrcEnblR10 to be less X sensitive.
Rearrange hardware ifetch access physical address forcing to not force
gvaR8R9 input fullswing so can be halfswing to handle new run to ICC.
tst/spy.V: Eta spys were counting in wrong direction.
cj/Makefile: Add rsrvdedepi.tst rule.
yy/tas.pl: Deposit/withdraw & copyswap had obsolete opcode-number assignments.
[ife,cj,tst]/*rst.tst tst/drvchk.V: update to match other recent changes.
ife/iffree.tst: Earlier new reset PC experiments had broken.
=====

```

```

RCS file: /s6/cvsroot/euterpe/doc/BOM,v
Working file: doc/BOM
head: 22.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 70;    selected revisions: 1
description:
BOM for doc
-----

```

```

revision 19.2
date: 1995/04/11 23:18:49; author: bobm; state: Exp; lines: +12 -12
Release Target: euterpe/doc
    euterpe-microarch.book
    front.mif
    euterpe-microarchTOC.mif
    intro.mif
    opcodes.mif
    xlu.mif
    pipeline.mif
    memory.mif
    events.mif
    reset.mif
    cerberus.mif
    newchanges.mif

```

```

Release of version 1.8 of Euterpe MicroArchitecture. There are some
changes to this version, but basically I'm releasing it before
incorporating review changes.
=====

```

```

RCS file: /s6/cvsroot/euterpe/doc/Attic/cerberus.mif,v
Working file: doc/cerberus.mif
head: 4.39
branch:
locks: strict
access list:

```

```
keyword substitution: kv
total revisions: 53;    selected revisions: 2
description:
-----
revision 4.30
date: 1995/04/12 23:06:49;  author: bobm;  state: Exp;  lines: +104 -251
Added info on backdoor ROM access.
-----
revision 4.29
date: 1995/04/11 23:09:46;  author: bobm;  state: Exp;  lines: +644 -279
pre-review release.
=====
```

```
RCS file: /s6/cvsroot/euterpe/doc/Attic/euterpe-microarch.book,v
Working file: doc/euterpe-microarch.book
head: 4.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 22;    selected revisions: 1
description:
-----
```

```
revision 4.9
date: 1995/04/11 23:15:50;  author: bobm;  state: Exp;  lines: +17 -16
pre-review release
=====
```

```
RCS file: /s6/cvsroot/euterpe/doc/Attic/events.mif,v
Working file: doc/events.mif
head: 4.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 28;    selected revisions: 1
description:
-----
```

```
revision 4.17
date: 1995/04/11 23:09:24;  author: bobm;  state: Exp;  lines: +46 -33
pre-review release.
=====
```

```
RCS file: /s6/cvsroot/euterpe/doc/Attic/front.mif,v
Working file: doc/front.mif
head: 16.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 2
description:
-----
```

```
revision 16.5
date: 1995/04/11 23:15:53;  author: bobm;  state: Exp;  lines: +27 -27
pre-review release
=====
```

revision 16.4
date: 1995/04/11 23:06:55; author: bobm; state: Exp; lines: +26 -26
pre-review release.
=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/intro.mif,v
Working file: doc/intro.mif
head: 4.22
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 26; selected revisions: 1
description:

revision 4.16
date: 1995/04/11 23:07:02; author: bobm; state: Exp; lines: +655 -156
pre-review release.
=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/memory.mif,v
Working file: doc/memory.mif
head: 4.36
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 46; selected revisions: 2
description:

revision 4.27
date: 1995/04/12 23:06:18; author: bobm; state: Exp; lines: +260 -198
Added info on backdoor ROM access.

revision 4.26
date: 1995/04/11 23:09:00; author: bobm; state: Exp; lines: +856 -741
pre-review release.
=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/newchanges.mif,v
Working file: doc/newchanges.mif
head: 16.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13; selected revisions: 1
description:

revision 16.5
date: 1995/04/11 23:10:07; author: bobm; state: Exp; lines: +295 -39
pre-review release.
=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/opcodes.mif,v
Working file: doc/opcodes.mif
head: 4.24

```

branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 39;    selected revisions: 1
description:
-----
revision 4.18
date: 1995/04/11 23:07:22;  author: bobm;  state: Exp;  lines: +20 -20
pre-review release.
=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/pipeline.mif,v
Working file: doc/pipeline.mif
head: 4.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 27;    selected revisions: 1
description:
-----
revision 4.16
date: 1995/04/11 23:08:36;  author: bobm;  state: Exp;  lines: +144 -144
pre-review release.
=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/reset.mif,v
Working file: doc/reset.mif
head: 4.22
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 26;    selected revisions: 1
description:
-----
revision 4.16
date: 1995/04/11 23:09:31;  author: bobm;  state: Exp;  lines: +89 -25
pre-review release.
=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/verify.html,v
Working file: doc/verify.html
head: 18.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 2
description:
-----
revision 18.13
date: 1995/04/13 18:50:56;  author: djc;   state: Exp;  lines: +2 -1
Added addr_map_mc
-----
revision 18.12

```


date: 1995/04/11 23:57:42; author: djc; state: Exp; lines: +2 -1
added addr_map_hermes

=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/xlu.mif,v
Working file: doc/xlu.mif
head: 4.21
branch:

locks: strict
access list:
keyword substitution: kv
total revisions: 29; selected revisions: 1
description:

revision 4.21

date: 1995/04/11 23:08:23; author: bobm; state: Exp; lines: +41 -299
pre-review release.

=====

RCS file: /s6/cvsroot/euterpe/verify/BOM,v
Working file: verify/BOM
head: 12.34

branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 404; selected revisions: 4
description:

revision 4.91

date: 1995/04/13 21:06:36; author: doi; state: Exp; lines: +2 -2
Release Target: euterpe/verify/ukernel

used the _real_boot instead of boot_pl_kernel by mistake

revision 4.90

date: 1995/04/10 22:42:23; author: doi; state: Exp; lines: +4 -4
Release Target: euterpe/verify

Makefile
Makefile.rules
Makefile.defs

Makefile: Changed and added some targets for dummy_boot.
Makefile.rules: Got rid of %.rom rule and moved it into verify/Makefile.rules
Makefile.defs: Added definition for mergesections tool.
Removed paths to nanoboot, boot, ukernel, etc. and put them
into verify/Makefile.rules.

revision 4.89

date: 1995/04/10 22:35:31; author: doi; state: Exp; lines: +2 -2
Release Target: euterpe/verify/tools

new mergesections tool

revision 4.88

date: 1995/04/10 22:31:06; author: doi; state: Exp; lines: +2 -2

Release Target: euterpe/verify/ukernel

time for a rebuild

=====

RCS file: /s6/cvsroot/euterpe/verify/Makefile.defs,v

Working file: verify/Makefile.defs

head: 1.43

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 43; selected revisions: 1

description:

revision 1.36

date: 1995/04/10 19:14:57; author: doi; state: Exp; lines: +2 -1

add definition for mergesections tool

=====

RCS file: /s6/cvsroot/euterpe/verify/obj/processor/inst/Makefile,v

Working file: verify/obj/processor/inst/Makefile

head: 1.182

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 182; selected revisions: 1

description:

revision 1.141

date: 1995/04/14 00:18:35; author: jeffm; state: Exp; lines: +2 -2

New test. Hangs hwterp.

=====

RCS file: /s6/cvsroot/euterpe/verify/tools/BOM,v

Working file: verify/tools/BOM

head: 13.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 90; selected revisions: 2

description:

releasebom adding BOM

revision 6.0

date: 1995/04/10 22:35:20; author: doi; state: Exp; lines: +1 -1

Release Target: euterpe/verify/tools

new mergesections tool

revision 5.11

date: 1995/04/10 22:35:13; author: doi; state: Exp; lines: +7 -9

releasebom: File needs to be up-to-date to use commit -r

```

RCS file: /s6/cvsroot/euterpe/verify/tools/ld/realld,v
Working file: verify/tools/ld/realld
head: 19.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 19.2
date: 1995/04/12 19:11:12;  author: jeffm;  state: Exp;  lines: +3 -3
Moved start vectors to offset x200.
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Makefile,v
Working file: verify/toplevel/Makefile
head: 1.185
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 185;    selected revisions: 1
description:
-----
revision 1.141
date: 1995/04/14 00:18:35;  author: jeffm;  state: Exp;  lines: +2 -2
New test. Hangs hwterp.
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/cache_debug.sig,v
Working file: verify/toplevel/cache_debug.sig
head: 33.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;      selected revisions: 1
description:
-----
revision 33.4
date: 1995/04/13 16:58:02;  author: jeffm;  state: Exp;  lines: +4 -1
Added signals for debugging icache_except.
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Attic/cachenasty.S,v
Working file: verify/toplevel/cachenasty.S
head: 33.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;      selected revisions: 1
description:
-----
revision 33.4
date: 1995/04/14 00:33:30;  author: jeffm;  state: Exp;  lines: +2 -2

```

Lisa Repka found a gtlb protection setup mistake. Was treating one of the intended dcache aliases as uncached.

=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Attic/cachenasty2.S,v
Working file: verify/toplevel/cachenasty2.S
head: 33.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5; selected revisions: 1
description:

revision 33.4
date: 1995/04/14 00:33:34; author: jeffm; state: Exp; lines: +2 -2
Lisa Repka found a gtlb protection setup mistake. Was treating one of the intended dcache aliases as uncached.

=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Attic/cachesynchnasty.S,v
Working file: verify/toplevel/cachesynchnasty.S
head: 35.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5; selected revisions: 2
description:

revision 35.2
date: 1995/04/14 00:33:38; author: jeffm; state: Exp; lines: +2 -2
Lisa Repka found a gtlb protection setup mistake. Was treating one of the intended dcache aliases as uncached.

revision 35.1
date: 1995/04/14 00:18:32; author: jeffm; state: Exp;
New test. Hangs hwterp.

=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/ex11test3.S,v
Working file: verify/toplevel/ex11test3.S
head: 35.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4; selected revisions: 2
description:

revision 35.4
date: 1995/04/12 19:34:13; author: jeffm; state: Exp; lines: +3 -3
Fixed two more cases. Passes hwterp.

revision 35.3
date: 1995/04/11 21:55:53; author: jeffm; state: Exp; lines: +36 -1
Fix exception return addresses for the ifetch exception cases.

```

=====
RCS file: /s6/cvsroot/euterpe/verify/toplevel/icacheharder3.S,v
Working file: verify/toplevel/icacheharder3.S
head: 33.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
-----
revision 33.3
date: 1995/04/12 23:14:15; author: jeffm; state: Exp; lines: +80 -18
Added case for priv >= XA priv.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verify/ukernel/BOM,v
Working file: verify/ukernel/BOM
head: 8.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;     selected revisions: 4
description:
releasebom adding BOM
-----
revision 4.0
date: 1995/04/13 21:06:23; author: doi; state: Exp; lines: +1 -1
Release Target: euterpe/verify/ukernel

```

used the `_real_boot` instead of `boot_pl_kernel` by mistake

```

-----
revision 3.1
date: 1995/04/13 21:06:16; author: doi; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
-----
revision 3.0
date: 1995/04/10 22:30:55; author: doi; state: Exp; lines: +1 -1
Release Target: euterpe/verify/ukernel

```

time for a rebuild

```

-----
revision 2.1
date: 1995/04/10 22:30:48; author: doi; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

```

```

RCS file: /s6/cvsroot/euterpe/verify/ukernel/Makefile,v
Working file: verify/ukernel/Makefile
head: 1.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;     selected revisions: 1

```

```

description:
-----
revision 1.6
date: 1995/04/13 21:05:35; author: doi; state: Exp; lines: +22 -16
used the wrong _real_ boot instead of boot_pl_kernel
=====

RCS file: /s6/cvsroot/euterpe/verilog/BOM,v
Working file: verilog/BOM
head: 6.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1390; selected revisions: 17
description:
top level verilog BOM
-----
revision 3.473
date: 1995/04/13 23:49:30; author: woody; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

uu:
Update placement to latest version. Still bigger than geert wants. Using some
of the 4 rows above the reg file.
uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the
4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx timmg fix.

cp:
disable an internal mapping of cerberus space to flash rom.
this function is only allowed by an external master poking at location '0'
location '0' and '1' boot from local rom.
all others boot over cerberus to master at location '0'

might be others
-----
revision 3.472
date: 1995/04/13 21:14:00; author: geert; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
Makefile.share

Changed number of iterations to 2

Geert
-----
revision 3.471
date: 1995/04/13 07:01:49; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc

move mc to the rigth 12 rows
-----
revision 3.470
date: 1995/04/13 06:55:46; author: dickson; state: Exp; lines: +2 -2

```

Release Target: euterpe/verilog/bsrc/es

remove another 12atoms in width

revision 3.469

date: 1995/04/12 23:15:04; author: dickson; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/ctiod

timing fix

revision 3.468

date: 1995/04/12 20:19:47; author: mws; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

rg/rgpc.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:

Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.

ALL (almost all) TESTS WILL NEED TO BE RECOMPILED.

Placement is not affected.

revision 3.467

date: 1995/04/12 16:17:00; author: billz; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/cc

Since the latest placement, hasn't made it into the latest bsrc/BOM,
(276.2) I'm releasing now.

revision 3.466

date: 1995/04/12 04:08:29; author: woody; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/lt

Added flop in snkReq path. This allows the signal from GT to be half-swing and
should fix the timing problem.

revision 3.465

date: 1995/04/12 03:58:58; author: woody; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/at

Added cdMissR12 to UvldStrR13/*UvldDcachStrR13*/. The dtag dirty bit was being
set by a store that gets a cache Miss. Test synch_1 noticed. Now it will only
write dirty bit if there was a cache hit.

revision 3.464

date: 1995/04/12 03:29:46; author: mws; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

rg/rgpc.V rg/rg.V rgxmit/rgxmit.V uu/uu.V euterpe.V \

rg/rg.pim rgxmit/rgxmit_control.pim:

Eliminate midpipe undo increment feature by moving predicted br inc
suppression controls backward in pipe. Saves muxff2_62 (a strip at
least 7 atoms wide 434 atoms total) and associated metal4.

uu/gen_mem.pl uu/uu_drive.V: Update reserved xlu instr tests to drive X's
in the register number fields when possible.

uu/uumic.tst: Add a predicted taken blinki case.

tst/job.tst: r[abc] and op[abc] &OpPreps done before \$RDst stuff ready.

cdio/cdio.V: Was copying the low datain to high datain for the 2nd half of
the CD write cycle.

revision 3.463
date: 1995/04/12 01:35:52; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/gf

timing fix

revision 3.462
date: 1995/04/11 18:58:34; author: woody; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

Fix typo.

revision 3.461
date: 1995/04/11 17:18:35; author: woody; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

Add flop in ltDone path to make it half-swing.

revision 3.460
date: 1995/04/11 07:44:03; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

Noncrashing placements for rg, au (no change), rgxmit, lt, at.
This leaves just uu, ife, and icc yet to place.
Also grab new veena reserved instr tests in uu.

revision 3.459
date: 1995/04/10 19:52:22; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/es

move es to right more redid some alms and summation instruction changes

revision 3.458
date: 1995/04/10 19:47:03; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc

move mc to the right

revision 3.457
date: 1995/04/09 10:41:49; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

HEAD FOR THE HILLS -- This is a huge change. Placements coming later.
Main pipe PC was updated too late on branches to be used on trgt ITag mtch.
Tests tlb_1 and probably any unix notice.
Main pipe PL was updated too late on branches to be used on trgt ITag mtch.
Even worse, it was way too late for LTLB to check br adrs on behalf of trgt.
Found by inspection, maybe icache_except might notice.
rg/rgpc.V rg/rg.V euterpe.V:
Delete pcr3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprb1mr5.Vegn uu/uuprb1mr7.Vegn uu/uu.V euterpe.V:
Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
icc/icc.V icc/icc_control.pim euterpe.V:
Add 5 stage shift register & snapper so ICC can capture a gva[63:48] on
branches and thus no longer need to continous ltlb of its own and so it
can get high gva in time for use on target.


```

icc/icc.V icc/icc_control.pim: Pipe for plR4 was 1 stage too short causing
cylinders to use others' priv levels. Probably is mostly responsible for
test icache except failure, but see bsrc/euterpe.status for another FL bug.
ife/ife.V ife/ifpcsel1l.Veqn: Merge ifp sel & ciRdNdx muxes in I2 stage
by getting rid of tag index mux fanin on ciRdNdx.
ife/ife.V ife/ifpcsel1l.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe
and snapped miss gva [47:12] to ICC so all in uniform place and to cut
control back & forth.
ife/ife.V: Detect mispredict recovery to sequential new
page & request corresponding hiccup to check protection. Found by inspection;
sinister protection implications if were not found.
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg???.pim:
Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
Delete pc[63:48] sent to for ICC's version of ltlb translation.
Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.
at/atpaselgen8.Veqn (delete) at/atpaselgen8.V (add) at/Makefile:
Reimplement so that gva input can be halfswing to handle new run to ICC.
at/at.V: Reorder dor pins into UfrcEnblR10 to be less X sensitive.
Rearrange hardware ifetch access physical address forcing to not force
gvaR8R9 input fullswing so can be halfswing to handle new run to ICC.
tst/spy.V: Eta spys were counting in wrong direction.
cj/Makefile: Add rsrvdedepl.tst rule.
yy/tas.pl: Deposit/withdraw & copyswap had obsolete opcode-number assignments.
{ife,cj,tst}/*rst.tst tst/drvchk.V: update to match other recent changes.
ife/iffree.tst: Earlier new reset PC experiments had broken.
=====

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/BOM,v

Working file: verilog/bsrc/BOM

head: 346.6

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 1737; selected revisions: 22

description:

revision 278.0

date: 1995/04/13 23:49:11; author: woody; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

uu:

Update placement to latest version. Still bigger than geert wants. Using some of the 4 rows above the reg file.

uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the 4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx timng fix.

cp:

disable an internal mapping of cerberus space to flash rom.

this function is only allowed by an external master poking at location '0'

location '0' and '1' boot from local rom.

all others boot over cerberus to master at location '0'

might be others

revision 277.5

date: 1995/04/13 23:48:59; author: woody; state: Exp; lines: +26 -26

releasebom: File needs to be up-to-date to use commit -r

revision 277.4

date: 1995/04/13 21:13:33; author: geert; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

Makefile.share

Changed number of iterations to 2

Geert

revision 277.3

date: 1995/04/13 07:01:24; author: dickson; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/mc

move mc to the rigth 12 rows

revision 277.2

date: 1995/04/13 06:55:20; author: dickson; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/es

remove another 12atoms in width

revision 277.1

date: 1995/04/12 23:14:47; author: dickson; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/ctiod

timing fix

revision 277.0

date: 1995/04/12 20:19:29; author: mws; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

rg/rgpc.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:

Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.

ALL (almost all) TESTS WILL NEED TO BE RECOMPILED.

Placement is not affected.

revision 276.4

date: 1995/04/12 20:19:16; author: mws; state: Exp; lines: +7 -7

releasebom: File needs to be up-to-date to use commit -r

revision 276.3

date: 1995/04/12 16:16:39; author: billz; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/cc

Since the latest placement, hasn't made it into the latest bsrc/BOM,
(276.2) I'm releasing now.

revision 276.2

date: 1995/04/12 04:08:11; author: woody; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/lt

Added flop in snkReq path. This allows the signal from GT to be half-swing and should fix the timing problem.

revision 276.1
date: 1995/04/12 03:58:41; author: woody; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

Added cdMissR12 to UvldStrR13/*UvldDcachStrR13*/. The dtag dirty bit was being set by a store that gets a cache Miss. Test synch_1 noticed. Now it will only write dirty bit if there was a cache hit.

revision 276.0
date: 1995/04/12 03:29:27; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

rg/rgpc.V rg/rg.V rgxmit/rgxmit.V uu/uu.V euterpe.V \
rg/rg.pim rgxmit/rgxmit_control.pim:
Eliminate midpipe undo increment feature by moving predicted br inc
suppression controls backward in pipe. Saves muxff2_62 (a strip at
least 7 atoms wide 434 atoms total) and associated metal4.
uu/gen_mem.pl uu/uu_drive.V: Update reserved xlu instr tests to drive X's
in the register number fields when possible.
uu/uumic.tst: Add a predicted taken blinki case.
tst/job.tst: r[abc] and op[abc] &OpPreps done before \$RDst stuff ready.
cdio/cdio.V: Was copying the low datain to high datain for the 2nd half of
the CD write cycle.

revision 275.4
date: 1995/04/12 03:29:15; author: mws; state: Exp; lines: +17 -17
releasebom: File needs to be up-to-date to use commit -r

revision 275.3
date: 1995/04/12 01:35:34; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/gf

timing fix

revision 275.2
date: 1995/04/11 18:58:11; author: woody; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

Fix typo.

revision 275.1
date: 1995/04/11 17:18:16; author: woody; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

Add flop in ltDone path to make it half-swing.

revision 275.0
date: 1995/04/11 07:43:41; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

Noncrashing placements for rg, au (no change), rgxmit, lt, at.
This leaves just uu, ife, and icc yet to place.
Also grab new veena reserved instr tests in uu.

```

revision 274.3
date: 1995/04/11 07:43:25; author: mws; state: Exp; lines: +8 -8
releasebm: File needs to be up-to-date to use commit -r
-----
revision 274.2
date: 1995/04/10 19:52:06; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/es

move es to right more redid some alms and summation instruction changes
-----
revision 274.1
date: 1995/04/10 19:46:46; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc

move mc to the right
-----
revision 274.0
date: 1995/04/09 10:41:30; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

HEAD FOR THE HILLS -- This is a huge change. Placements coming later.
Main pipe PC was updated too late on branches to be used on trgt ITag mtch.
Tests tlbl_1 and probably any unix notice.
Main pipe FL was updated too late on branches to be used on trgt ITag mtch.
Even worse, it was way too late for LTLB to check br adrs on behalf of trgt.
Found by inspection, maybe icache_except might notice.
rg/rgpc.V rg/rg.V euterpe.V:
Delete pcr3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
icc/icc.V icc/icc_control.pim euterpe.V:
Add 5 stage shift register & snapper so ICC can capture a gva[63:48] on
branches and thus no longer need to continous tlbl of its own and so it
can get high gva in time for use on target.
icc/icc.V icc/icc_control.pim: Pipe for plR4 was 1 stage too short causing
cylinders to use others' priv levels. Probably is mostly responsible for
test icache except failure, but see bsrc/euterpe.status for another FL bug.
ife/ife.V ife/ifpcselil.Veqn: Merge ifp sel & ciRdNdx muxes in I2 stage
by getting rid of tag index mux fanin on ciRdNdx.
ife/ife.V ife/ifpcselil.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe
and snapped miss gva [47:12] to ICC so all in uniform place and to cut
control back & forth.
ife/ife.V: Detect mispredict recovery to sequential new
page & request corresponding hiccup to check protection. Found by inspection;
sinister protection implications if were not found.
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg???.pim:
Delete tlbl xor data formerly sent to ICC so that it could do own xlation.
Delete pc[63:48] sent to for ICC's version of tlbl translation.
Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.
at/atpaselgen8.Veqn (delete) at/atpaselgen8.V (add) at/Makefile:
Reimplement so that gva input can be halfswing to handle new run to ICC.
at/at.V: Reorder dor pins into UfrcEnblR10 to be less X sensitive.
Rearrange hardware ifetch access physical address forcing to not force
gvaR8R9 input fullswing so can be halfswing to handle new run to ICC.
tst/spy.V: Eta spys were counting in wrong direction.
cj/Makefile: Add rsrvdedepl.tst rule.

```

```
yy/tas.pl: Deposit/withdraw & copyswap had obsolete opcode-number assignments.
{ife,cj,tst}/*rst.tst tst/drvchk.V: update to match other recent changes.
ife/iffree.tst: Earlier new reset PC experiments had broken.
```

```
-----
revision 273.2
date: 1995/04/09 10:41:18; author: mws; state: Exp; lines: +15 -15
releasebom: File needs to be up-to-date to use commit -r
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile,v
Working file: verilog/bsrc/Makefile
head: 1.255
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 255; selected revisions: 1
description:
-----
```

```
revision 1.231
date: 1995/04/09 15:58:43; author: lisar; state: Exp; lines: +17 -3
Added creation of hermes files to simfiles target
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.share,v
Working file: verilog/bsrc/Makefile.share
head: 1.57
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 57; selected revisions: 1
description:
-----
```

```
revision 1.53
date: 1995/04/13 21:12:40; author: geert; state: Exp; lines: +2 -2
Changed number of iterations to 2
Geert
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.tst,v
Working file: verilog/bsrc/Makefile.tst
head: 40.104
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 104; selected revisions: 11
description:
-----
```

```
revision 40.66
date: 1995/04/13 22:42:15; author: chip; state: Exp; lines: +3 -3
Changed routing order for XLU result bus and aundx wire
```

```
Geert
-----
```

```
revision 40.65
```

```

date: 1995/04/13 22:11:30; author: chip; state: Exp; lines: +4 -4
CVFixed an error in the pim.rev generation

: -----
-----
revision 40.64
date: 1995/04/13 21:26:09; author: geert; state: Exp; lines: +2 -2
topt.new -> TOPT_PROG

Geert
-----
revision 40.63
date: 1995/04/13 21:15:15; author: geert; state: Exp; lines: +21 -11
Changes soem stuff related to generation of pim files
from previous pof files for iterations

GHeert
-----
revision 40.62
date: 1995/04/12 18:28:50; author: chip; state: Exp; lines: +2 -2
Added a dependency from the netlits to the gplace.lis

Geert
-----
revision 40.61
date: 1995/04/11 17:45:43; author: chip; state: Exp; lines: +1 -2
Nothing major

Geert

ZZ
-----
revision 40.60
date: 1995/04/11 17:45:12; author: geert; state: Exp; lines: +3 -3
Changed adependency

Geert
-----
revision 40.59
date: 1995/04/10 20:03:20; author: chip; state: Exp; lines: +5 -5
More cleaning up
-----
revision 40.58
date: 1995/04/10 18:23:53; author: chip; state: Exp; lines: +15 -12
I fixed the iteration rules so that we can easily
restart from the middle rather than have it start from the
top all the time
-----
revision 40.57
date: 1995/04/10 05:01:03; author: chip; state: Exp; lines: +2 -2
Fixed a typo .. I got the
top-level iteration stuff working now..

Geert
-----
revision 40.56
date: 1995/04/10 02:29:34; author: chip; state: Exp; lines: +5 -4

```

Fixed a bug in .pof.pif.pim

Geert
`

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.vo,v

Working file: verilog/bsrc/Makefile.vo

head: 27.45

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 45; selected revisions: 8

description:

revision 27.28

date: 1995/04/12 17:26:06; author: chip; state: Exp; lines: +2 -2

Small bug-fix needs tabs instaed of spaces before

xlu noflip rules

geert

revision 27.27

date: 1995/04/12 16:58:50; author: vo; state: Exp; lines: +2 -1

Added xlu cells to list of critical cells to prevent them from getting flipped .

revision 27.26

date: 1995/04/11 20:11:17; author: chip; state: Exp; lines: +2 -2

Fixed a bug related to the GASTATUS step

Geert

revision 27.25

date: 1995/04/11 19:29:05; author: chip; state: Exp; lines: +2 -2

Fixed a bug introduced by the last change (rsh \$(GARDS-HOST))

revision 27.24

date: 1995/04/11 19:22:56; author: chip; state: Exp; lines: +3 -3

Got ridf of the srh to godzilla

Geert

revision 27.23

date: 1995/04/11 18:54:06; author: geert; state: Exp; lines: +2 -2

Another bug fix related to the \$*. *234 files

Geert

revision 27.22

date: 1995/04/11 18:48:54; author: chip; state: Exp; lines: +2 -2

No major changes

formatting stuff

Geert

```

revision 27.21
date: 1995/04/11 18:48:24; author: geert; state: Exp; lines: +4 -7
Fixed a bug in the *243 files. Need to be prefixed
by chipname

Geert
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/c_euterpe_wrap.parm,v
Working file: verilog/bsrc/c_euterpe_wrap.parm
head: 183.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;      selected revisions: 1
description:
-----
revision 183.7
date: 1995/04/09 05:11:47; author: lisar; state: Exp; lines: +16 -16
Add memory init files for hermes devices.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/clockbias.hwc,v
Working file: verilog/bsrc/clockbias.hwc
head: 35.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;      selected revisions: 1
description:
-----
revision 35.7
date: 1995/04/10 18:23:06; author: chip; state: Exp; lines: +1 -19
I took out the unused nets so that HWCROUTE does not die
anymore

Geert
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.V,v
Working file: verilog/bsrc/euterpe.V
head: 6.431
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 431;    selected revisions: 5
description:
-----
revision 6.397
date: 1995/04/13 03:35:21; author: dickson; state: Exp; lines: +2 -2
removed gndzro from cp interface as we on converge on
our boot sequence.
-----
revision 6.396

```


date: 1995/04/13 00:10:08; author: dickson; state: Exp; lines: +19 -13
extra copy of auindx output for hz and sr
timing fix for CCrstUT
timing fix for AUTauUW

revision 6.395

date: 1995/04/12 20:04:31; author: billz; state: Exp; lines: +4 -4
NBwed change. NBwed is generated one cycle earlier.
Becomes NBwedX0 at top level.

revision 6.394

date: 1995/04/12 03:08:12; author: mws; state: Exp; lines: +19 -19
rg/rgpc.V rg/rg.V rgxmit/rgxmit.V uu/uu.V euterpe.V \
rg/rg.pim rgxmit/rgxmit_control.pim:

Eliminate midpipe undo increment feature by moving predicted br inc
suppression controls backward in pipe. Saves muxff2_62 (a strip at
least 7 atoms wide 434 atoms total) and associated metal4.

revision 6.393

date: 1995/04/09 09:58:02; author: mws; state: Exp; lines: +97 -127
rg/rgpc.V rg/rg.V euterpe.V:

Delete pcR3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcpn.
icc/icc.V icc/icc_control.pim euterpe.V:

Add 5 stage shift register & snapper so ICC can capture a gva[63:48] on
branches and thus no longer need to continous lt1b of its own and so it
can get high gva in time for use on target.
ife/ife.V ife/ifpcsel11.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe
and snapped miss gva [47:12] to ICC so all in uniform place and to cut
control back & forth.

lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg??pim:

Delete lt1b xor data formerly sent to ICC so that it could do own xlation.

Delete pc[63:48] sent to for ICC's version of lt1b translation.

Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.status,v

Working file: verilog/bsrc/euterpe.status

head: 24.83

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 83; selected revisions: 6

description:

revision 24.56

date: 1995/04/12 20:00:48; author: mws; state: Exp; lines: +3 -2
Add note on global access control proposal.

rg/rgpc.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:

Change reset PC from 0000_0000_0000 to 0000_4000_0000_0200.

revision 24.55

date: 1995/04/12 03:21:19; author: mws; state: Exp; lines: +6 -5
Reflect recent fixes.

```

-----
revision 24.54
date: 1995/04/11 17:17:43; author: mws; state: Exp; lines: +1 -4
Reflect cdio high write data in hold for 4 ticks fix.
-----
revision 24.53
date: 1995/04/11 07:23:38; author: mws; state: Exp; lines: +57 -50
Catching up.
-----
revision 24.52
date: 1995/04/09 10:24:15; author: mws; state: Exp; lines: +2 -39
Delete entries for a number of fixed bugs.
-----
revision 24.51
date: 1995/04/09 09:56:53; author: mws; state: Exp; lines: +24 -1
Main pipe PC updated too late on branches to be used on trgt ITag mtch.
    Tests tlb_1 and probably any unix notice.
Main pipe PL updated too late on branches to be used on trgt ITag mtch.
    Even worse, it was way too late for LTLB to check br adrs on behalf of trgt.
    Found by inspection, maybe icache_except might notice.
More silly logic.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe_wrap.V,v
Working file: verilog/bsrc/euterpe_wrap.V
head: 15.104
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 104;    selected revisions: 2
description:
-----
revision 15.91
date: 1995/04/12 03:14:28; author: lisar; state: Exp; lines: +14 -46
Added force of pok for pll1.

Yuck Yuck Yuck
Caught out by the ancient forces of cerberus for running the hermes channels.
-----
revision 15.90
date: 1995/04/09 10:36:33; author: mws; state: Exp; lines: +3 -3
    Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/genpim2.pl,v
Working file: verilog/bsrc/genpim2.pl
head: 41.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 1
description:
-----
revision 41.14
date: 1995/04/08 18:23:56; author: chip; state: Exp; lines: +2 -5

```

I took out the last off-set for cc

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/padtiles.ercf,v

Working file: verilog/bsrc/padtiles.ercf

head: 168.8

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 8; selected revisions: 2

description:

revision 168.3

date: 1995/04/10 23:58:25; author: geert; state: Exp; lines: +2 -2

Route early nets in order

Geert

revision 168.2

date: 1995/04/10 18:31:23; author: chip; state: Exp; lines: +9 -0

Fixed the routing strategy so that it generates a %.garout.lis
file

Geert

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/BOM,v

Working file: verilog/bsrc/at/BOM

head: 93.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 184; selected revisions: 6

description:

releasebom adding BOM

revision 69.0

date: 1995/04/12 03:58:21; author: woody; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc/at

Added cdMissR12 to UvldStrR13/*UvldDcachStrR13*/. The dtag dirty bit was being
set by a store that gets a cache Miss. Test synch_1 noticed. Now it will only
write dirty bit if there was a cache hit.

revision 68.1

date: 1995/04/12 03:58:12; author: woody; state: Exp; lines: +3 -3

releasebom: File needs to be up-to-date to use commit -r

revision 68.0

date: 1995/04/11 07:26:40; author: mws; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

Noncrashing placements for rg, au (no change), rgxmit, lt, at.
This leaves just uu, ife, and icc yet to place.

```

revision 67.1
date: 1995/04/11 07:26:32; author: mws; state: Exp; lines: +7 -8
releasecom: File needs to be up-to-date to use commit -r
-----
revision 67.0
date: 1995/04/09 10:26:11; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

HEAD FOR THE HILLS -- This is a huge change. Placements coming later.
Main pipe PC was updated too late on branches to be used on trgt ITag mtch.
  Tests tlb_1 and probably any uniX notice.
Main pipe PL was updated too late on branches to be used on trgt ITag mtch.
  Even worse, it was way too late for LTLB to check br adrs on behalf of trgt.
  Found by inspection, maybe icache_except might notice.
rg/rgpc.V rg/rg.V euterpe.V:
  Delete pcr3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
  Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcpn.
icc/icc.V icc/icc_control.pim euterpe.V:
  Add 5 stage shift register & snapper so ICC can capture a gva[63:48] on
  branches and thus no longer need to continous ltlb of its own and so it
  can get high gva in time for use on target.
icc/icc.V icc/icc_control.pim: Pipe for plR4 was 1 stage too short causing
  cylinders to use others' priv levels. Probably is mostly responsible for
  test icache_except failure, but see bsrc/euterpe.status for another PL bug.
ife/ife.V ife/ifpcsel1.Veqn: Merge ifp sel & ciRdNdx muxes in I2 stage
  by getting rid of tag index mux fanin on ciRdNdx.
ife/ife.V ife/ifpcsel1.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe
  and snapped miss gva [47:12] to ICC so all in uniform place and to cut
  control back & forth.
ife/ife.V: Detect mispredict recovery to sequential new
  page & request corresponding hiccup to check protection. Found by inspection;
  sinister protection implications if were not found.
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg???.pim:
  Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
  Delete pc[63:48] sent to for ICC's version of ltlb translation.
  Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.
at/atpaselgen8.Veqn (delete) at/atpaselgen8.V (add) at/Makefile:
  Reimplement so that gva input can be halfswing to handle new run to ICC.
at/at.V: Reorder dor pins into UfrcEnblR10 to be less X sensitive.
  Rearrange hardware ifetch access physical address forcing to not force
  gvaR8R9 input fullswing so can be halfswing to handle new run to ICC.
tst/spy.V: Eta spys were counting in wrong direction.
cj/Makefile: Add rsrvdedepl.tst rule.
yy/tas.pl: Deposit/withdraw & copyswap had obsolete opcode-number assignments.
{ife,cj,tst}/*rst.tst tst/drvchk.V: update to match other recent changes.
ife/iffree.tst: Earlier new reset PC experiments had broken.
-----
revision 66.1
date: 1995/04/09 10:26:04; author: mws; state: Exp; lines: +4 -4
releasecom: File needs to be up-to-date to use commit -r
-----
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/Makefile,v
Working file: verilog/bsrc/at/Makefile
head: 1.18

```

```

branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 18;    selected revisions: 2
description:
-----
revision 1.16
date: 1995/04/11 04:22:31; author: mws; state: Exp; lines: +2 -2
at/at.V at/atpaselgen64.V at/atpaselgen8.V:
    Shorten instance names to gards limit.
at/atpaselgen64.V at/atpaselgen2.Veqn(delete) at/Makefile:
    Make bits 7:6 same halfswing style as 63:6, but by using pruning, so that
    standard module atpaselgen8 can be reused.
-----
revision 1.15
date: 1995/04/09 09:42:19; author: mws; state: Exp; lines: +3 -3
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
    Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
at/atpaselgen8.Veqn (delete) at/atpaselgen8.V (add) at/Makefile:
    Reimplement so that gva input can be halfswing to handle new run to ICC.
at/at.V: Reorder dor pins into UfrcEnblR10 to be less X sensitive.
    Rearrange hardware ifetch access physical address forcing to not force
    gvaR8R9 input fullswing so can be halfswing to handle new run to ICC.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/at.V,v
Working file: verilog/bsrc/at/at.V
head: 1.66
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 66;    selected revisions: 3
description:
-----
revision 1.50
date: 1995/04/12 03:51:31; author: woody; state: Exp; lines: +3 -3
Added cdMissR12 to UvldStrR13/*UvldDcachStrR13*/. The dtag dirty bit was being
set by a store that gets a cache Miss. Test synch_1 noticed.

5woody fabbed.
-----
revision 1.49
date: 1995/04/11 04:22:32; author: mws; state: Exp; lines: +13 -13
at/at.V at/atpaselgen64.V at/atpaselgen8.V:
    Shorten instance names to gards limit.
at/atpaselgen64.V at/atpaselgen2.Veqn(delete) at/Makefile:
    Make bits 7:6 same halfswing style as 63:6, but by using pruning, so that
    standard module atpaselgen8 can be reused.
-----
revision 1.48
date: 1995/04/09 09:42:22; author: mws; state: Exp; lines: +26 -19
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
    Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.

```

```

at/atpaselgen8.Veqn (delete) at/atpaselgen8.V (add) at/Makefile:
  Reimplement so that gva input can be halfswing to handle new run to ICC.
at/at.V:  Reorder dor pins into UfrcEnblR10 to be less X sensitive.
  Rearrange hardware ifetch access physical address forcing to not force
  gvaR8R9 input fullswing so can be halfswing to handle new run to ICC.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/at.pim,v
Working file: verilog/bsrc/at/at.pim
head: 51.23
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 23;    selected revisions: 1
description:
=====

```

```

revision 51.8
date: 1995/04/11 04:22:13;  author: mws;  state: Exp;  lines: +199 -179
at/at.V at/atpaselgen64.V at/atpaselgen8.V:
  Shorten instance names to gards limit.
at/atpaselgen64.V at/atpaselgen2.Veqn(delete) at/Makefile:
  Make bits 7:6 same halfswing style as 63:6, but by using pruning, so that
  standard module atpaselgen8 can be reused.
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
  Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
at/atpaselgen8.Veqn (delete) at/atpaselgen8.V (add) at/Makefile:
  Reimplement so that gva input can be halfswing to handle new run to ICC.
at/at.V:  Reorder dor pins into UfrcEnblR10 to be less X sensitive.
  Rearrange hardware ifetch access physical address forcing to not force
  gvaR8R9 input fullswing so can be halfswing to handle new run to ICC.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/at.power.tab.top,v
Working file: verilog/bsrc/at/at.power.tab.top
head: 28.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;    selected revisions: 1
description:
=====

```

```

revision 28.7
date: 1995/04/10 19:57:17;  author: chip;  state: Exp;  lines: +1417 -1721
new top-level io powerfile
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/atpaselgen64.V,v
Working file: verilog/bsrc/at/atpaselgen64.V
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;    selected revisions: 1

```

description:

revision 1.3

date: 1995/04/11 04:22:34; author: mws; state: Exp; lines: +17 -13

at/at.V at/atpaselgen64.V at/atpaselgen8.V:

Shorten instance names to gards limit.

at/atpaselgen64.V at/atpaselgen2.Veqn(delete) at/Makefile:

Make bits 7:6 same halfswing style as 63:6, but by using pruning, so that
standard module atpaselgen8 can be reused.

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/atpaselgen8.V,v

Working file: verilog/bsrc/at/atpaselgen8.V

head: 66.2

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 2; selected revisions: 2

description:

revision 66.2

date: 1995/04/11 04:22:35; author: mws; state: Exp; lines: +3 -3

at/at.V at/atpaselgen64.V at/atpaselgen8.V:

Shorten instance names to gards limit.

at/atpaselgen64.V at/atpaselgen2.Veqn(delete) at/Makefile:

Make bits 7:6 same halfswing style as 63:6, but by using pruning, so that
standard module atpaselgen8 can be reused.

revision 66.1

date: 1995/04/09 09:42:23; author: mws; state: Exp;

rg/rqpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \

icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:

Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
at/atpaselgen8.Veqn (delete) at/atpaselgen8.V (add) at/Makefile:

Reimplement so that gva input can be halfswing to handle new run to ICC.
at/at.V: Reorder dor pins into UfrcEnblR10 to be less X sensitive.

Rearrange hardware ifetch access physical address forcing to not force

gvaR8R9 input fullswing so can be halfswing to handle new run to ICC.

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/genpim.pl,v

Working file: verilog/bsrc/at/genpim.pl

head: 3.12

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 12; selected revisions: 1

description:

revision 3.11

date: 1995/04/11 21:02:59; author: chip; state: Exp; lines: +2 -2

Moved orgin a bit to the left

Geert
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/BOM,v

Working file: verilog/bsrc/au/BOM

head: 44.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 89; selected revisions: 4

description:

revision 35.0

date: 1995/04/13 23:38:26; author: woody; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

uu:

Update placement to latest version. Still bigger than geert wants. Using some of the 4 rows above the reg file.

uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the 4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx timing fix.

cp:

disable an internal mapping of cerberus space to flash rom.

this function is only allowed by an external master poking at location '0'

location '0' and '1' boot from local rom.

all others boot over cerberus to master at location '0'

might be others

revision 34.1

date: 1995/04/13 23:38:20; author: woody; state: Exp; lines: +3 -3

releasebom: File needs to be up-to-date to use commit -r

revision 34.0

date: 1995/04/09 10:26:29; author: mws; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

HEAD FOR THE HILLS -- This is a huge change. Placements coming later.

Main pipe PC was updated too late on branches to be used on trgt ITag mtch.

Tests tlb_1 and probably any unix notice.

Main pipe PL was updated too late on branches to be used on trgt ITag mtch.

Even worse, it was way too late for LTLB to check br adrs on behalf of trgt.

Found by inspection, maybe icache_except might notice.

rg/rgpc.V rg/rg.V euterpe.V:

Delete pcr3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.

rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \

icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:

Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.

icc/icc.V icc/icc_control.pim euterpe.V:

Add 5 stage shift register & snapper so ICC can capture a gva[63:48] on

branches and thus no longer need to continous ltlb of its own and so it

can get high gva in time for use on target.

icc/icc.V icc/icc_control.pim: Pipe for plR4 was 1 stage too short causing


```

cylinders to use others' priv levels. Probably is mostly responsible for
test icache_except failure, but see bsrc/euterpe.status for another PL bug.
ife/ife.V ife/ifpcseli1.Veqn: Merge ifp sel & ciRdNdx muxes in I2 stage
by getting rid of tag index mux fanin on ciRdNdx.
ife/ife.V ife/ifpcseli1.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe
and snapped miss gva [47:12] to ICC so all in uniform place and to cut
control back & forth.
ife/ife.V: Detect mispredict recovery to sequential new
page & request corresponding hiccup to check protection. Found by inspection;
sinister protection implications if were not found.
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg??pim:
Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
Delete pc[63:48] sent to for ICC's version of ltlb translation.
Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.
at/atpaselgen8.Veqn (delete) at/atpaselgen8.V (add) at/Makefile:
Reimplement so that gva input can be halfswing to handle new run to ICC.
at/at.V: Reorder dor pins into UfrcEnb1R10 to be less X sensitive.
Rearrange hardware ifetch access physical address forcing to not force
gvaR8R9 input fullswing so can be halfswing to handle new run to ICC.
tst/spy.V: Eta spys were counting in wrong direction.
cj/Makefile: Add rsrvdedepi.tst rule.
yy/tas.pl: Deposit/withdraw & copyswap had obsolete opcode-number assignments.
{ife,cj,tst}/*rst.tst tst/drvchk.V: update to match other recent changes.
ife/iffree.tst: Earlier new reset PC experiments had broken.

```

```

-----
revision 33.1

```

```

date: 1995/04/09 10:26:22; author: mws; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r

```

```

-----
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/au.power.tab.top,v
Working file: verilog/bsrc/au/au.power.tab.top
head: 16.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11; selected revisions: 1
description:

```

```

-----
revision 16.8
date: 1995/04/10 19:57:23; author: chip; state: Exp; lines: +148 -164
new top-level io powerfile

```

```

-----
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/auindx.V,v
Working file: verilog/bsrc/au/auindx.V
head: 1.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 24; selected revisions: 2
description:

```

```

-----
revision 1.22
date: 1995/04/12 23:50:29; author: dickson; state: Exp; lines: +19 -2

```

make buffered copy of output address to solve timing problem at top level.

revision 1.21

date: 1995/04/09 09:43:44; author: mws; state: Exp; lines: +9 -7

rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \

icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:

Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/BOM,v

Working file: verilog/bsrc/cc/BOM

head: 92.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 182; selected revisions: 4

description:

releasebom adding BOM

revision 77.0

date: 1995/04/13 23:38:47; author: woody; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

uu:

Update placement to latest version. Still bigger than geert wants. Using some of the 4 rows above the reg file.

uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the 4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx timng fix.

cp:

disable an internal mapping of cerberus space to flash rom.

this function is only allowed by an external master poking at location '0'

location '0' and '1' boot from local rom.

all others boot over cerberus to master at location '0'

might be others

revision 76.1

date: 1995/04/13 23:38:40; author: woody; state: Exp; lines: +3 -3

releasebom: File needs to be up-to-date to use commit -r

revision 76.0

date: 1995/04/12 16:16:18; author: billz; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc/cc

Since the latest placement, hasn't made it into the latest bsrc/BOM,
(276.2) I'm releasing now.

revision 75.1

date: 1995/04/12 16:16:10; author: billz; state: Exp; lines: +4 -4

releasebom: File needs to be up-to-date to use commit -r

=====

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cc.power.tab.top,v
Working file: verilog/bsrc/cc/cc.power.tab.top
head: 32.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;      selected revisions: 1
description:
-----
revision 32.5
date: 1995/04/10 19:57:26;  author: chip;  state: Exp;  lines: +644 -522
new top-level io powerfile
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/genpim.pl,v
Working file: verilog/bsrc/cc/genpim.pl
head: 5.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;      selected revisions: 1
description:
-----
revision 5.15
date: 1995/04/11 20:57:20;  author: chip;  state: Exp;  lines: +2 -2
Fixed the origin to 491 from 494

```

Geert

=====

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cdio/BOM,v
Working file: verilog/bsrc/cdio/BOM
head: 55.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 110;      selected revisions: 4
description:
releasebom adding BOM
-----
revision 47.0
date: 1995/04/13 23:39:07;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

```

uu:

Update placement to latest version. Still bigger than geert wants. Using some of the 4 rows above the reg file.

uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the 4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx timng fix.

```
cp:
  disable an internal mapping of cerberus space to flash rom.
  this function is only allowed by an external master poking at location '0'
  location '0' and '1' boot from local rom.
  all others boot over cerberus to master at location '0'
```

might be others

```
-----
revision 46.1
date: 1995/04/13 23:39:01; author: woody; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
-----
```

```
revision 46.0
date: 1995/04/12 03:22:02; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc
```

```
rg/rgpc.V rg/rg.V rgxmit/rgxmit.V uu/uu.V euterpe.V \
rg/rg.pim rgxmit/rgxmit_control.pim:
```

```
  Eliminate midpipe undo increment feature by moving predicted br inc
  suppression controls backward in pipe. Saves muxff2_62 (a strip at
  least 7 atoms wide 434 atoms total) and associated metal4.
uu/gen_mem.pl uu/uu_drive.V: Update reserved xlu instr tests to drive X's
  in the register number fields when possible.
uu/uumic.tst: Add a predicted taken blinki case.
tst/job.tst: r[abc] and op[abc] &OpPreps done before $RDst stuff ready.
cdio/cdio.V: Was copying the low datain to high datain for the 2nd half of
  the CD write cycle.
```

```
-----
revision 45.1
date: 1995/04/12 03:21:55; author: mws; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cdio/cdio.power.tab.top,v
Working file: verilog/bsrc/cdio/cdio.power.tab.top
head: 34.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
-----
```

```
revision 34.8
date: 1995/04/10 19:57:31; author: chip; state: Exp; lines: +75 -75
new top-level io powerfile
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/BOM,v
Working file: verilog/bsrc/ce/BOM
head: 86.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 170;    selected revisions: 2
```

```

description:
releasebom adding BOM
-----
revision 74.0
date: 1995/04/13 23:39:29; author: woody; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu:
Update placement to latest version. Still bigger than geert wants. Using some
of the 4 rows above the reg file.
uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the
4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx timng fix.

cp:
disable an internal mapping of cerberus space to flash rom.
this function is only allowed by an external master poking at location '0'
location '0' and '1' boot from local rom.
all others boot over cerberus to master at location '0'

might be others
-----
revision 73.1
date: 1995/04/13 23:39:23; author: woody; state: Exp; lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/BOM,v
Working file: verilog/bsrc/cj/BOM
head: 122.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 259; selected revisions: 6
description:
-----
revision 112.0
date: 1995/04/12 20:09:24; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

rg/rgpc.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:
Change reset PC from 0000 4000 0000 0000 to 0000 4000 0000 0200.
ALL NONIBUFFER-STARTING TESTS WILL NEED TO BE RECOMPILED.
Placement is not affected.
-----
revision 111.1
date: 1995/04/12 20:09:14; author: mws; state: Exp; lines: +11 -11
releasebom: File needs to be up-to-date to use commit -r
-----
revision 111.0
date: 1995/04/12 03:22:37; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

```

-

```

rg/rgpc.V rg/rg.V rgxmit/rgxmit.V uu/uu.V euterpe.V \
rg/rg.pim rgxmit/rgxmit_control.pim:
    Eliminate midpipe undo increment feature by moving predicted br inc
    suppression controls backward in pipe. Saves muxff2_62 (a strip at
    least 7 atoms wide 434 atoms total) and associated metal4.
uu/gen_mem.pl uu/uu_drive.V: Update reserved xlu instr tests to drive X's
    in the register number fields when possible.
uu/uumic.tst: Add a predicted taken blinki case.
tst/job.tst: r[abc] and op[abc] & OpPreps done before $RDst stuff ready.
cdio/cdio.V: Was copying the low datain to high datain for the 2nd half of
    the CD write cycle.
-----
revision 110.1
date: 1995/04/12 03:22:30; author: mws; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
-----
revision 110.0
date: 1995/04/09 10:27:13; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

HEAD FOR THE HILLS -- This is a huge change. Placements coming later.
Main pipe PC was updated too late on branches to be used on trgt ITag mtch.
    Tests tlbb_1 and probably any unix notice.
Main pipe FL was updated too late on branches to be used on trgt ITag mtch.
    Even worse, it was way too late for LTLB to check br adrs on behalf of trgt.
    Found by inspection, maybe icache_except might notice.
rg/rgpc.V rg/rg.V euterpe.V:
    Delete pcR3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
    Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
icc/icc.V icc/icc_control.pim euterpe.V:
    Add 5 stage shift register & snapper so ICC can capture a gva[63:48] on
    branches and thus no longer need to continous ltlb of its own and so it
    can get high gva in time for use on target.
icc/icc.V icc/icc_control.pim: Pipe for plR4 was 1 stage too short causing
    cylinders to use others' priv levels. Probably is mostly responsible for
    test icache_except failure, but see bsrc/euterpe.status for another FL bug.
ife/ife.V ife/ifpcselil.Veqn: Merge ifp sel & ciRdNdx muxes in I2 stage
    by getting rid of tag index mux fanin on ciRdNdx.
ife/ife.V ife/ifpcselil.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe
    and snapped miss gva [47:12] to ICC so all in uniform place and to cut
    control back & forth.
ife/ife.V: Detect mispredict recovery to sequential new
    page & request corresponding hiccup to check protection. Found by inspection;
    sinister protection implications if were not found.
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg???.pim:
    Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
    Delete pc[63:48] sent to for ICC's version of ltlb translation.
    Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.
at/atpaselgen8.Veqn (delete) at/atpaselgen8.V (add) at/Makefile:
    Reimplement so that gva input can be halfswing to handle new run to ICC.
at/at.V: Reorder dor pins into UfrcEnblR10 to be less X sensitive.
    Rearrange hardware ifetch access physical address forcing to not force
    gvaR8R9 input fullswing so can be halfswing to handle new run to ICC.
tst/spy.V: Eta spys were counting in wrong direction.
cj/Makefile: Add rsrvdedepl.tst rule.

```

```
yy/tas.pl: Deposit/withdraw & copyswap had obsolete opcode-number assignments.
{ife,cj,tst}/*rst.tst tst/drvchk.V: update to match other recent changes.
ife/iffree.tst: Earlier new reset PC experiments had broken.
```

```
-----
revision 109.1
```

```
date: 1995/04/09 10:27:06; author: mws; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
```

```
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/br.tst,v
```

```
Working file: verilog/bsrc/cj/br.tst
```

```
head: 2.15
```

```
branch:
```

```
locks: strict
```

```
access list:
```

```
keyword substitution: kv
```

```
total revisions: 15; selected revisions: 1
```

```
description:
```

```
-----
revision 2.14
```

```
date: 1995/04/12 20:01:07; author: mws; state: Exp; lines: +24 -22
```

```
rg/rnpc.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:
```

```
Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.
```

```
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/cj.power.tab.top,v
```

```
Working file: verilog/bsrc/cj/cj.power.tab.top
```

```
head: 69.12
```

```
branch:
```

```
locks: strict
```

```
access list:
```

```
keyword substitution: kv
```

```
total revisions: 12; selected revisions: 1
```

```
description:
```

```
-----
revision 69.11
```

```
date: 1995/04/10 19:57:35; author: chip; state: Exp; lines: +349 -299
```

```
new top-level io powerfile
```

```
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/cjrst.tst,v
```

```
Working file: verilog/bsrc/cj/cjrst.tst
```

```
head: 13.39
```

```
branch:
```

```
locks: strict
```

```
access list:
```

```
keyword substitution: kv
```

```
total revisions: 39; selected revisions: 1
```

```
description:
```

```
-----
revision 13.34
```

```
date: 1995/04/09 09:44:19; author: mws; state: Exp; lines: +3 -3
```

```
{ife,cj,tst}/*rst.tst tst/drvchk.V: update to match other recent changes.
```

```
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/freel.tst,v
```

```
Working file: verilog/bsrc/cj/freel.tst
```

```

head: 1.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
Pipe some instructions through front end pipe with no issue holds.
A tstgen test with stride==1.
=====
revision 1.10
date: 1995/04/12 20:01:09; author: mws; state: Exp; lines: +11 -10
rg/rGPC.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:
Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/hic.tst,v
Working file: verilog/bsrc/cj/hic.tst
head: 11.21
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 21;    selected revisions: 1
description:
=====
revision 11.20
date: 1995/04/12 20:01:10; author: mws; state: Exp; lines: +2 -2
rg/rGPC.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:
Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/hold.tst,v
Working file: verilog/bsrc/cj/hold.tst
head: 1.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
Pipe some instructions through front end pipe with some issue holds.
A tstgen test with stride==5.
=====
revision 1.15
date: 1995/04/12 20:01:12; author: mws; state: Exp; lines: +20 -19
rg/rGPC.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:
Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/ifbr.tst,v
Working file: verilog/bsrc/cj/ifbr.tst
head: 3.20
branch:
locks: strict
access list:
keyword substitution: kv

```



```

total revisions: 20;    selected revisions: 1
description:
-----
revision 3.19
date: 1995/04/12 20:01:14; author: mws; state: Exp; lines: +40 -37
rg/rGPC.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:
    Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/ifpred3-11.tst,v
Working file: verilog/bsrc/cj/ifpred3-11.tst
head: 23.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;    selected revisions: 1
description:
-----
revision 23.8
date: 1995/04/12 20:01:16; author: mws; state: Exp; lines: +33 -32
rg/rGPC.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:
    Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/ifpred3-2.tst,v
Working file: verilog/bsrc/cj/ifpred3-2.tst
head: 20.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;    selected revisions: 1
description:
-----
revision 20.7
date: 1995/04/12 20:01:18; author: mws; state: Exp; lines: +28 -27
rg/rGPC.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:
    Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/micbr.tst,v
Working file: verilog/bsrc/cj/micbr.tst
head: 5.27
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 27;    selected revisions: 1
description:
-----
revision 5.26
date: 1995/04/12 20:01:19; author: mws; state: Exp; lines: +2 -3
rg/rGPC.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:
    Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/pcbhnd.tst,v
Working file: verilog/bsrc/cj/pcbhnd.tst
head: 5.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16;    selected revisions: 2
description:
-----
revision 5.15
date: 1995/04/12 20:01:21; author: mws; state: Exp; lines: +3 -3
rg/rgpc.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:
    Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.
-----

```

```

revision 5.14
date: 1995/04/12 03:16:15; author: mws; state: Exp; lines: +6 -6
Add some debugging job0-9 callouts & comments.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/rsrvd.tst,v
Working file: verilog/bsrc/cj/rsrvd.tst
head: 78.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 1
description:
-----
revision 78.9
date: 1995/04/12 20:01:22; author: mws; state: Exp; lines: +2 -2
rg/rgpc.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:
    Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ck/BOM,v
Working file: verilog/bsrc/ck/BOM
head: 26.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 50;    selected revisions: 2
description:
releasebom adding BOM
-----

```

```

revision 24.0
date: 1995/04/13 23:40:03; author: woody; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

```

```

uu:
    Update placement to latest version. Still bigger than geert wants. Using some
    of the 4 rows above the reg file.
    uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the
    4 rows for powering up without running in to ES.

```

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx timng fix.

cp:

disable an internal mapping of cerberus space to flash rom.
this function is only allowed by an external master poking at location '0'
location '0' and '1' boot from local rom.
all others boot over cerberus to master at location '0'

might be others

revision 23.1

date: 1995/04/13 23:39:56; author: woody; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ck/ck.power.tab.top,v

Working file: verilog/bsrc/ck/ck.power.tab.top

head: 17.8

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 8; selected revisions: 1

description:

revision 17.7

date: 1995/04/10 19:57:38; author: chip; state: Exp; lines: +78 -40

new top-level io powerfile

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/BOM,v

Working file: verilog/bsrc/cp/BOM

head: 60.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 119; selected revisions: 2

description:

releasebom adding BOM

revision 49.0

date: 1995/04/13 23:40:23; author: woody; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

uu:

Update placement to latest version. Still bigger than geert wants. Using some
of the 4 rows above the reg file.

uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the
4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx timng fix.

```
cp:
  disable an internal mapping of cerberus space to flash rom.
  this function is only allowed by an external master poking at location '0'
  location '0' and '1' boot from local rom.
  all others boot over cerberus to master at location '0'
```

might be others

```
-----
revision 48.1
date: 1995/04/13 23:40:16; author: woody; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/cp.V,v
Working file: verilog/bsrc/cp/cp.V
head: 1.39
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 39; selected revisions: 1
description:
-----
```

```
revision 1.32
date: 1995/04/13 03:29:56; author: dickson; state: Exp; lines: +12 -28
disable an internal mapping of cerberus space to flash rom.
this function is only allowed by an external master poking at
location '0'
location '0' and '1' boot from local rom.
all others boot over cerberus to master at location '0'
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/cp.power.tab.top,v
Working file: verilog/bsrc/cp/cp.power.tab.top
head: 19.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12; selected revisions: 1
description:
-----
```

```
revision 19.8
date: 1995/04/10 19:57:41; author: chip; state: Exp; lines: +159 -155
new top-level io powerfile
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctiod/BOM,v
Working file: verilog/bsrc/ctiod/BOM
head: 31.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 61; selected revisions: 2
description:
releasebom adding BOM
```

```
-----  
revision 25.0  
date: 1995/04/12 23:14:29; author: dickson; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc/ctiod
```

```
timing fix  
-----
```

```
revision 24.1  
date: 1995/04/12 23:14:22; author: dickson; state: Exp; lines: +3 -3  
releasebom: File needs to be up-to-date to use commit -r  
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctiod/ctiod.power.tab.top,v  
Working file: verilog/bsrc/ctiod/ctiod.power.tab.top  
head: 12.8  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 8; selected revisions: 1  
description:  
-----
```

```
revision 12.7  
date: 1995/04/10 19:57:44; author: chip; state: Exp; lines: +13 -11  
new top-level io powerfile  
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctiod/genptab.pl,v  
Working file: verilog/bsrc/ctiod/genptab.pl  
head: 1.9  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 9; selected revisions: 1  
description:  
-----
```

```
revision 1.6  
date: 1995/04/12 23:13:49; author: dickson; state: Exp; lines: +4 -4  
change power levels from 4s to 6s for muxff2_32dinlo/muxff2_16dinhi  
to solve timing problems  
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctioi/BOM,v  
Working file: verilog/bsrc/ctioi/BOM  
head: 28.0  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 56; selected revisions: 2  
description:  
releasebom adding BOM  
-----
```

```
revision 24.0  
date: 1995/04/13 23:40:48; author: woody; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc
```

uu:
Update placement to latest version. Still bigger than geert wants. Using some
of the 4 rows above the reg file.
uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the
4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx: timng fix.

cp:
disable an internal mapping of cerberus space to flash rom.
this function is only allowed by an external master poking at location '0'
location '0' and '1' boot from local rom.
all others boot over cerberus to master at location '0'

might be others

revision 23.1

date: 1995/04/13 23:40:42; author: woody; state: Exp; lines: +2 -2

releasebom: File needs to be up-to-date to use commit -r

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctioi/ctioi.power.tab.top,v

Working file: verilog/bsrc/ctioi/ctioi.power.tab.top

head: 9.9

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 9; selected revisions: 1

description:

revision 9.8

date: 1995/04/10 19:57:46; author: chip; state: Exp; lines: +26 -24

new top-level io powerfile

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dp/BOM,v

Working file: verilog/bsrc/dp/BOM

head: 45.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 91; selected revisions: 2

description:

releasebom adding BOM

revision 45.0

date: 1995/04/13 23:41:08; author: woody; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

uu:
Update placement to latest version. Still bigger than geert wants. Using some
of the 4 rows above the reg file.

uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the 4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx timng fix.

cp:

disable an internal mapping of cerberus space to flash rom.
this function is only allowed by an external master poking at location '0'
location '0' and '1' boot from local rom.
all others boot over cerberus to master at location '0'

might be others

revision 44.1

date: 1995/04/13 23:41:01; author: woody; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/BOM,v

Working file: verilog/bsrc/dr/BOM

head: 77.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 155; selected revisions: 2

description:

releasebom adding BOM
=====

revision 69.0

date: 1995/04/13 23:41:53; author: woody; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

uu:

Update placement to latest version. Still bigger than geert wants. Using some of the 4 rows above the reg file.

uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the 4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx timng fix.

cp:

disable an internal mapping of cerberus space to flash rom.
this function is only allowed by an external master poking at location '0'
location '0' and '1' boot from local rom.
all others boot over cerberus to master at location '0'

might be others

revision 68.1

date: 1995/04/13 23:41:46; author: woody; state: Exp; lines: +2 -2

releasebom: File needs to be up-to-date to use commit -r
=====

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/dr.power.tab.top,v
Working file: verilog/bsrc/dr/dr.power.tab.top
head: 43.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;      selected revisions: 1
description:
-----
revision 43.5
date: 1995/04/10 19:57:50;  author: chip;  state: Exp;  lines: +1495 -1557
new top-level io powerfile
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/drio/BOM,v
Working file: verilog/bsrc/drio/BOM
head: 26.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 50;      selected revisions: 2
description:
releasebom adding BOM
-----

```

```

revision 18.0
date: 1995/04/13 23:42:12;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

```

```

uu:
  Update placement to latest version. Still bigger than geert wants. Using some
  of the 4 rows above the reg file.
  uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the
  4 rows for powering up without running in to ES.

```

```

nb,uu, euterpe.V: nbWeDX1 timing fix.

```

```

au: auindx timng fix.

```

```

cp:
  disable an internal mapping of cerberus space to flash rom.
  this function is only allowed by an external master poking at location '0'
  location '0' and '1' boot from local rom.
  all others boot over cerberus to master at location '0'

```

```

might be others
-----

```

```

revision 17.1
date: 1995/04/13 23:42:05;  author: woody;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/drio/drio.power.tab.top,v
Working file: verilog/bsrc/drio/drio.power.tab.top
head: 9.11

```



```

branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
-----
revision 9.7
date: 1995/04/10 19:57:55;  author: chip;  state: Exp;  lines: +32 -32
new top-level io powerfile
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/BOM,v
Working file: verilog/bsrc/es/BOM
head: 97.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 198;    selected revisions: 4
description:
-----
revision 86.0
date: 1995/04/13 06:54:53;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/es

remove another 12atoms in width
-----
revision 85.1
date: 1995/04/13 06:54:43;  author: dickson;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
-----
revision 85.0
date: 1995/04/10 19:51:47;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/es

move es to right more redid some alms and summation instruction changes
-----
revision 84.1
date: 1995/04/10 19:51:40;  author: dickson;  state: Exp;  lines: +6 -6
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/clean-request,v
Working file: verilog/bsrc/es/clean-request
head: 45.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
-----
revision 45.14
date: 1995/04/10 19:49:42;  author: dickson;  state: Exp;  lines: +2 -1
squeeze es more.
alms ans summation instruction layout changed.

```

a minor logic design change for alms instruction
to help routability.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/es.V,v
Working file: verilog/bsrc/es/es.V

head: 5.46

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 46; selected revisions: 1

description:

revision 5.44

date: 1995/04/10 19:49:44; author: dickson; state: Exp; lines: +5 -5
squeeze es more.

alms ans summation instruction layout changed.

a minor logic design change for alms instruction
to help routability.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/es.pim,v

Working file: verilog/bsrc/es/es.pim

head: 5.55

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 55; selected revisions: 1

description:

revision 5.48

date: 1995/04/10 19:49:59; author: dickson; state: Exp; lines: +7337 -7332
squeeze es more.

alms ans summation instruction layout changed.

a minor logic design change for alms instruction
to help routability.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/es.power.tab.top,v

Working file: verilog/bsrc/es/es.power.tab.top

head: 65.12

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 12; selected revisions: 1

description:

revision 65.10

date: 1995/04/10 19:58:07; author: chip; state: Exp; lines: +1766 -1748
new top-level io powerfile

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/esalmsum.V,v

Working file: verilog/bsrc/es/esalmsum.V

```

head: 60.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;      selected revisions: 1
description:
-----
revision 60.5
date: 1995/04/10 19:50:13; author: dickson; state: Exp; lines: +32 -28
squeeze es more.
alms ans summation instruction layout changed.
a minor logic design change for alms instruction
to help routability.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/esalmsumb.V,v
Working file: verilog/bsrc/es/esalmsumb.V
head: 60.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;      selected revisions: 1
description:
-----
revision 60.4
date: 1995/04/10 19:50:15; author: dickson; state: Exp; lines: +7 -8
squeeze es more.
alms ans summation instruction layout changed.
a minor logic design change for alms instruction
to help routability.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gf/BOM,v
Working file: verilog/bsrc/gf/BOM
head: 37.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 72;     selected revisions: 2
description:
releasebom adding BOM
-----
revision 31.0
date: 1995/04/12 01:35:16; author: dickson; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/gf

```

```

timing fix
-----
revision 30.1
date: 1995/04/12 01:35:09; author: dickson; state: Exp; lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gf/clean-request,v

```

```

Working file: verilog/bsrc/gf/clean-request
head: 11.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;      selected revisions: 1
description:
-----
revision 11.7
date: 1995/04/12 01:34:26;  author: dickson;  state: Exp;  lines: +1 -9
timing fix
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gf/gf.V,v
Working file: verilog/bsrc/gf/gf.V
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;      selected revisions: 1
description:
-----
revision 1.7
date: 1995/04/12 01:34:28;  author: dickson;  state: Exp;  lines: +12 -10
timing fix
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gf/gf.pim,v
Working file: verilog/bsrc/gf/gf.pim
head: 4.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;     selected revisions: 1
description:
-----
revision 4.11
date: 1995/04/12 01:34:31;  author: dickson;  state: Exp;  lines: +2 -0
timing fix
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gf/gf.power.tab.top,v
Working file: verilog/bsrc/gf/gf.power.tab.top
head: 19.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;      selected revisions: 1
description:
-----
revision 19.8
date: 1995/04/10 19:58:18;  author: chip;  state: Exp;  lines: +471 -471
new top-level io powerfile

```

```
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/.checkoutrc,v
Working file: verilog/bsrc/gt/.checkoutrc
head: 39.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;      selected revisions: 1
description:
-----
```

```
revision 39.4
date: 1995/04/11 17:17:21; author: woody; state: Exp; lines: +2 -2
set display to hard038:0.0
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/BOM,v
Working file: verilog/bsrc/gt/BOM
head: 98.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 194;    selected revisions: 4
description:
releasebom adding BOM
-----
```

```
revision 83.0
date: 1995/04/11 18:57:51; author: woody; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/gt
```

Fix typo.

```
-----
revision 82.1
date: 1995/04/11 18:57:42; author: woody; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
-----
revision 82.0
date: 1995/04/11 17:17:58; author: woody; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/gt
```

Add flop in ltDone path to make it half-swing.

```
-----
revision 81.1
date: 1995/04/11 17:17:50; author: woody; state: Exp; lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/gt.power.tab.top,v
Working file: verilog/bsrc/gt/gt.power.tab.top
head: 54.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;     selected revisions: 1
```

```

description:
-----
revision 54.8
date: 1995/04/10 19:58:23; author: chip; state: Exp; lines: +391 -393
new top-level io powerfile
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/gtsnake.V,v
Working file: verilog/bsrc/gt/gtsnake.V
head: 7.41
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 41; selected revisions: 1
description:
-----
revision 7.38
date: 1995/04/11 17:11:12; author: woody; state: Exp; lines: +5 -2
Add flop in ltDone path to make it half-swing.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/pimlib.pl,v
Working file: verilog/bsrc/gt/pimlib.pl
head: 26.23
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 23; selected revisions: 2
description:
-----
revision 26.16
date: 1995/04/11 18:57:12; author: woody; state: Exp; lines: +2 -2
Fix typo.
-----
revision 26.15
date: 1995/04/11 17:11:15; author: woody; state: Exp; lines: +2 -2
Add flop in ltDone path to make it half-swing.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/BOM,v
Working file: verilog/bsrc/hc/BOM
head: 125.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 250; selected revisions: 2
description:
releasebom adding BOM
-----
revision 102.0
date: 1995/04/13 23:42:57; author: woody; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu:

```

Update placement to latest version. Still bigger than geert wants. Using some of the 4 rows above the reg file.
uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the 4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx: timng fix.

cp:
disable an internal mapping of cerberus space to flash rom.
this function is only allowed by an external master poking at location '0'
location '0' and '1' boot from local rom.
all others boot over cerberus to master at location '0'

might be others

revision 101.1
date: 1995/04/13 23:42:48; author: woody; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc0.power.tab.top,v
Working file: verilog/bsrc/hc/hc0.power.tab.top
head: 68.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9; selected revisions: 1
description:

revision 68.6
date: 1995/04/10 19:58:28; author: chip; state: Exp; lines: +687 -701
new top-level io powerfile
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc1.power.tab.top,v
Working file: verilog/bsrc/hc/hc1.power.tab.top
head: 68.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9; selected revisions: 1
description:

revision 68.6
date: 1995/04/10 19:59:29; author: chip; state: Exp; lines: +555 -569
new top-level io powerfile
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hz/BOM,v
Working file: verilog/bsrc/hz/BOM
head: 30.0
branch:
locks: strict

```

access list:
keyword substitution: kv
total revisions: 58;      selected revisions: 2
description:
releasebom adding BOM
-----
revision 26.0
date: 1995/04/13 23:43:20;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu:
Update placement to latest version. Still bigger than geert wants. Using some
of the 4 rows above the reg file.
uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the
4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWedX1 timing fix.

au: auindx timng fix.

cp:
disable an internal mapping of cerberus space to flash rom.
this function is only allowed by an external master poking at location '0'
location '0' and '1' boot from local rom.
all others boot over cerberus to master at location '0'

might be others
-----
revision 25.1
date: 1995/04/13 23:43:13;  author: woody;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hz/hz.power.tab.top,v
Working file: verilog/bsrc/hz/hz.power.tab.top
head: 10.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;      selected revisions: 1
description:
-----
revision 10.6
date: 1995/04/10 20:00:54;  author: chip;  state: Exp;  lines: +112 -24
new top-level io powerfile
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/BOM,v
Working file: verilog/bsrc/icc/BOM
head: 49.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 96;      selected revisions: 6
description:

```


releasebom adding BOM

revision 39.0

date: 1995/04/13 23:43:45; author: woody; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu:

Update placement to latest version. Still bigger than geert wants. Using some of the 4 rows above the reg file.

uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the 4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx timng fix.

cp:

disable an internal mapping of cerberus space to flash rom.

this function is only allowed by an external master poking at location '0' location '0' and '1' boot from local rom.

all others boot over cerberus to master at location '0'

might be others

revision 38.1

date: 1995/04/13 23:43:37; author: woody; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r

revision 38.0

date: 1995/04/11 07:29:47; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

Noncrashing placements for rg, au (no change), rgxmit, lt, at.
This leaves just uu, ife, and icc yet to place.

revision 37.1

date: 1995/04/11 07:29:40; author: mws; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r

revision 37.0

date: 1995/04/09 10:29:07; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

HEAD FOR THE HILLS -- This is a huge change. Placements coming later.

Main pipe PC was updated too late on branches to be used on trgt ITag mtch.

Tests tlb 1 and probably any unix notice.

Main pipe PL was updated too late on branches to be used on trgt ITag mtch.

Even worse, it was way too late for LTLB to check br adrs on behalf of trgt.

Found by inspection, maybe icache_except might notice.

rg/rgpc.V rg/rg.V euterpe.V:

Delete pcr3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.

rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \

icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:

Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.

icc/icc.V icc/icc control.pim euterpe.V:

Add 5 stage shift register & snapper so ICC can capture a gva[63:48] on branches and thus no longer need to continous ltlb of its own and so it

```

    can get high gva in time for use on target.
icc/icc.V icc/icc_control.pim: Pipe for plR4 was 1 stage too short causing
cylinders to use others' priv levels. Probably is mostly responsible for
test icache except failure, but see bsrc/euterpe.status for another PL bug.
ife/ife.V ife/ifpcsel1l.Veqn: Merge ifp sel & ciRdNdx muxes in I2 stage
by getting rid of tag index mux fanin on ciRdNdx.
ife/ife.V ife/ifpcsel1l.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe
and snapped miss gva [47:12] to ICC so all in uniform place and to cut
control back & forth.
ife/ife.V: Detect mispredict recovery to sequential new
page & request corresponding hiccup to check protection. Found by inspection;
sinister protection implications if were not found.
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg???.pim:
Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
Delete pc[63:48] sent to for ICC's version of ltlb translation.
Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.
at/atpaselgen8.Veqn (delete) at/atpaselgen8.V (add) at/Makefile:
Reimplement so that gva input can be halfswing to handle new run to ICC.
at/at.V: Reorder dor pins into UfrcEnblR10 to be less X sensitive.
Rearrange hardware ifetch access physical address forcing to not force
gvaR8R9 input fullswing so can be halfswing to handle new run to ICC.
tst/spy.V: Eta spys were counting in wrong direction.
cj/Makefile: Add rsrvdedepi.tst rule.
yy/tas.pl: Deposit/withdraw & copyswap had obsolete opcode-number assignments.
[ife,cj,tst]/*rst.tst tst/drvchk.V: update to match other recent changes.
ife/iffree.tst: Earlier new reset PC experiments had broken.

```

```

revision 36.1

```

```

date: 1995/04/09 10:29:01; author: mws; state: Exp; lines: +3 -3

```

```

releasebom: File needs to be up-to-date to use commit -r

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/icc.V,v

```

```

Working file: verilog/bsrc/icc/icc.V

```

```

head: 1.45

```

```

branch:

```

```

locks: strict

```

```

access list:

```

```

keyword substitution: kv

```

```

total revisions: 45; selected revisions: 2

```

```

description:

```

```

revision 1.41

```

```

date: 1995/04/09 11:14:36; author: mws; state: Exp; lines: +19 -1

```

```

Add scalar wire declarations.

```

```

revision 1.40

```

```

date: 1995/04/09 09:52:54; author: mws; state: Exp; lines: +153 -157

```

```

rg/rgpc.V rg/rg.V euterpe.V:

```

```

Delete pcr3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.

```

```

rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprb1mr5.Veqn uu/uuprb1mr7.Veqn uu/uu.V euterpe.V:

```

```

Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
icc/icc.V icc/icc_control.pim euterpe.V:

```

```

Add 5 stage shift register & snapper so ICC can capture a gva[63:48] on
branches and thus no longer need to continous ltlb of its own and so it
can get high gva in time for use on target.

```

```

icc/icc.V icc/icc_control.pim: Pipe for plR4 was 1 stage too short causing
cylinders to use others' priv levels. Probably is mostly responsible for
test icache_except failure, but see bsrc/euterpe.status for another PL bug.
ife/ife.V ife/ifpcselil.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe
and snapped miss gva [47:12] to ICC so all in uniform place and to cut
control back & forth.
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg???.pim:
Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
Delete pc[63:48] sent to for ICC's version of ltlb translation.
Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/icc.power.tab.top,v
Working file: verilog/bsrc/icc/icc.power.tab.top
head: 19.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;      selected revisions: 1
description:
-----
revision 19.5
date: 1995/04/10 20:00:56; author: chip; state: Exp; lines: +145 -161
new top-level io powerfile
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/icc_control.pim,v
Working file: verilog/bsrc/icc/icc_control.pim
head: 16.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;      selected revisions: 1
description:
-----
revision 16.13
date: 1995/04/09 09:52:56; author: mws; state: Exp; lines: +54 -52
rg/rgpc.V rg/rg.V euterpe.V:
Delete pcr3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
icc/icc.V icc/icc_control.pim euterpe.V:
Add 5 stage shift register & snapper so ICC can capture a gva[63:48] on
branches and thus no longer need to continous ltlb of its own and so it
can get high gva in time for use on target.
icc/icc.V icc/icc_control.pim: Pipe for plR4 was 1 stage too short causing
cylinders to use others' priv levels. Probably is mostly responsible for
test icache_except failure, but see bsrc/euterpe.status for another PL bug.
ife/ife.V ife/ifpcselil.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe
and snapped miss gva [47:12] to ICC so all in uniform place and to cut
control back & forth.
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg???.pim:
Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
Delete pc[63:48] sent to for ICC's version of ltlb translation.

```

Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/BOM,v

Working file: verilog/bsrc/ife/BOM

head: 68.1

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 140; selected revisions: 4

description:

revision 61.0

date: 1995/04/12 20:15:24; author: mws; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

rg/rgpc.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uunic}.tst euterpe.status:

Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.

ALL (almost all) TESTS WILL NEED TO BE RECOMPILED.

Placement is not affected.

revision 60.1

date: 1995/04/12 20:11:37; author: mws; state: Exp; lines: +6 -6

releasebom: File needs to be up-to-date to use commit -r

revision 60.0

date: 1995/04/09 10:29:27; author: mws; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

HEAD FOR THE HILLS -- This is a huge change. Placements coming later.

Main pipe PC was updated too late on branches to be used on trgt ITag mtch.

Tests tlb_1 and probably any unix notice.

Main pipe PL was updated too late on branches to be used on trgt ITag mtch.

Even worse, it was way too late for LTLB to check br adrs on behalf of trgt.

Found by inspection, maybe icache_except might notice.

rg/rgpc.V rg/rg.V euterpe.V:

Delete pcr3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.

rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \

icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:

Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.

icc/icc.V icc/icc_control.pim euterpe.V:

Add 5 stage shift register & snapper so ICC can capture a gva[63:48] on

branches and thus no longer need to continous ltlb of its own and so it

can get high gva in time for use on target.

icc/icc.V icc/icc_control.pim: Pipe for plR4 was 1 stage too short causing

cylinders to use others' priv levels. Probably is mostly responsible for

test icache_except failure, but see bsrc/euterpe.status for another PL bug.

ife/ife.V ife/ifpcselil.Veqn: Merge ifp sel & ciRdNdx muxes in I2 stage

by getting rid of tag index mux fanin on ciRdNdx.

ife/ife.V ife/ifpcselil.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe

and snapped miss gva [47:12] to ICC so all in uniform place and to cut

control back & forth.

ife/ife.V: Detect mispredict recovery to sequential new

page & request corresponding hiccup to check protection. Found by inspection;

sinister protection implications if were not found.

lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg?.pim:

```

Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
Delete pc[63:48] sent to for ICC's version of ltlb translation.
Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.
at/atpaselgen8.Veqn (delete) at/atpaselgen8.V (add) at/Makefile:
Reimplement so that gva input can be halfswing to handle new run to ICC.
at/at.V: Reorder dor pins into UfrcEnblR10 to be less X sensitive.
Rearrange hardware ifetch access physical address forcing to not force
gvaR8R9 input fullswing so can be halfswing to handle new run to ICC.
tst/spy.V: Eta spys were counting in wrong direction.
cj/Makefile: Add rsrvdedepl.tst rule.
yy/tas.pl: Deposit/withdraw & copyswap had obsolete opcode-number assignments.
{ife,cj,tst}/*rst.tst tst/drvchk.V: update to match other recent changes.
ife/iffree.tst: Earlier new reset PC experiments had broken.
-----
revision 59.1
date: 1995/04/09 10:29:20; author: mws; state: Exp; lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/ifbr.tst,v
Working file: verilog/bsrc/ife/ifbr.tst
head: 1.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;      selected revisions: 1
description:
-----

```

```

revision 1.9
date: 1995/04/12 20:04:22; author: mws; state: Exp; lines: +74 -70
rg/rgpc.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uunic}.tst euterpe.status:
Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/ife.V,v
Working file: verilog/bsrc/ife/ife.V
head: 1.46
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 46;      selected revisions: 1
description:
-----

```

```

revision 1.42
date: 1995/04/09 09:53:30; author: mws; state: Exp; lines: +120 -108
ife/ife.V ife/ifpcsel11.Veqn: Merge ifp sel & ciRdNdx muxes in I2 stage
by getting rid of tag index mux fanin on ciRdNdx.
ife/ife.V ife/ifpcsel11.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe
and snapped miss gva [47:12] to ICC so all in uniform place and to cut
control back & forth.
ife/ife.V: Detect mispredict recovery to sequential new
page & request corresponding hiccup to check protection. Found by inspection;
sinister protection implications if were not found.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/ife.power.tab.top,v
Working file: verilog/bsrc/ife/ife.power.tab.top
head: 40.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;      selected revisions: 1
description:
-----
revision 40.4
date: 1995/04/10 20:00:59; author: chip; state: Exp; lines: +209 -201
new top-level io powerfile
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/iffree.tst,v
Working file: verilog/bsrc/ife/iffree.tst
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;      selected revisions: 2
description:
-----
revision 1.7
date: 1995/04/12 20:04:24; author: mws; state: Exp; lines: +2 -3
rg/rnpc.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:
    Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.
-----
revision 1.6
date: 1995/04/09 09:53:32; author: mws; state: Exp; lines: +10 -12
ife/ife.V ife/ifpcsel1l.Veqn: Merge ifp sel & ciRdNdx muxes in I2 stage
    by getting rid of tag index mux fanin on ciRdNdx.
ife/ife.V ife/ifpcsel1l.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe
    and snapped miss gva [47:12] to ICC so all in uniform place and to cut
    control back & forth.
ife/ife.V: Detect mispredict recovery to sequential new
    page & request corresponding hiccup to check protection. Found by inspection;
    sinister protection implications if were not found.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/iffree5.tst,v
Working file: verilog/bsrc/ife/iffree5.tst
head: 1.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;      selected revisions: 1
description:
-----
revision 1.5
date: 1995/04/12 20:04:26; author: mws; state: Exp; lines: +35 -36
rg/rnpc.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:
    Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/ifhold.tst,v
Working file: verilog/bsrc/ife/ifhold.tst
head: 1.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;      selected revisions: 1
description:
-----
revision 1.5
date: 1995/04/12 20:04:29; author: mws; state: Exp; lines: +30 -27
rg/rgpc.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,ummic}.tst euterpe.status:
Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/ifpcseli1.Veqn,v
Working file: verilog/bsrc/ife/ifpcseli1.Veqn
head: 1.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;      selected revisions: 1
description:
-----
revision 1.9
date: 1995/04/09 09:53:33; author: mws; state: Exp; lines: +5 -7
ife/ife.V ife/ifpcseli1.Veqn: Merge ifp sel & ciRdNdx muxes in I2 stage
by getting rid of tag index mux fanin on ciRdNdx.
ife/ife.V ife/ifpcseli1.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe
and snapped miss gva [47:12] to ICC so all in uniform place and to cut
control back & forth.
ife/ife.V: Detect mispredict recovery to sequential new
page & request corresponding hiccup to check protection. Found by inspection;
sinister protection implications if were not found.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/ifrst.tst,v
Working file: verilog/bsrc/ife/ifrst.tst
head: 2.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;     selected revisions: 1
description:
-----
revision 2.10
date: 1995/04/09 09:53:34; author: mws; state: Exp; lines: +2 -2
ife/ife.V ife/ifpcseli1.Veqn: Merge ifp sel & ciRdNdx muxes in I2 stage
by getting rid of tag index mux fanin on ciRdNdx.
ife/ife.V ife/ifpcseli1.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe
and snapped miss gva [47:12] to ICC so all in uniform place and to cut
control back & forth.
ife/ife.V: Detect mispredict recovery to sequential new

```

page & request corresponding hiccup to check protection. Found by inspection;
sinister protection implications if were not found.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/io/BOM,v
Working file: verilog/bsrc/io/BOM

head: 48.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 94; selected revisions: 2

description:

releasebom adding BOM

revision 41.0

date: 1995/04/13 23:44:23; author: woody; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

uu:

Update placement to latest version. Still bigger than geert wants. Using some
of the 4 rows above the reg file.

uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the
4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx timng fix.

cp:

disable an internal mapping of cerberus space to flash rom.

this function is only allowed by an external master poking at location '0'

location '0' and '1' boot from local rom.

all others boot over cerberus to master at location '0'

might be others

revision 40.1

date: 1995/04/13 23:44:15; author: woody; state: Exp; lines: +3 -3

releasebom: File needs to be up-to-date to use commit -r

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/io/io0.power.tab.top,v

Working file: verilog/bsrc/io/io0.power.tab.top

head: 24.8

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 8; selected revisions: 1

description:

revision 24.7

date: 1995/04/10 20:00:02; author: chip; state: Exp; lines: +118 -124

new top-level io powerfile


```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/io/iol.power.tab.top,v
Working file: verilog/bsrc/io/iol.power.tab.top
head: 24.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;    selected revisions: 1
description:
-----
revision 24.7
date: 1995/04/10 20:00:14;  author: chip;  state: Exp;  lines: +60 -66
new top-level io powerfile
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/iq/BOM,v
Working file: verilog/bsrc/iq/BOM
head: 67.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 145;  selected revisions: 2
description:
-----
revision 63.0
date: 1995/04/13 23:44:46;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

```

```

uu:
    Update placement to latest version. Still bigger than geert wants. Using some
    of the 4 rows above the reg file.
uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the
4 rows for powering up without running in to ES.

```

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx timng fix.

```

cp:
    disable an internal mapping of cerberus space to flash rom.
    this function is only allowed by an external master poking at location '0'
    location '0' and '1' boot from local rom.
    all others boot over cerberus to master at location '0'

```

might be others

```

-----
revision 62.1
date: 1995/04/13 23:44:39;  author: woody;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/iq/iq.power.tab.top,v
Working file: verilog/bsrc/iq/iq.power.tab.top
head: 50.6
branch:
locks: strict

```

```

access list:
keyword substitution: kv
total revisions: 6;      selected revisions: 1
description:
-----
revision 50.5
date: 1995/04/10 20:01:04;  author: chip;  state: Exp;  lines: +248 -1412
new top-level io powerfile
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/BOM,v
Working file: verilog/bsrc/lt/BOM
head: 98.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 196;   selected revisions: 6
description:
releasebom adding BOM
-----
revision 90.0
date: 1995/04/12 04:07:50;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/lt

Added flop in snkReq path. This allows the signal from GT to be half-swing and
should fix the timing problem.
-----
revision 89.1
date: 1995/04/12 04:07:41;  author: woody;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
-----
revision 89.0
date: 1995/04/11 07:30:31;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

Noncrashing placements for rg, au (no change), rgxmit, lt, at.
This leaves just uu, ife, and icc yet to place.
-----
revision 88.1
date: 1995/04/11 07:30:23;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
-----
revision 88.0
date: 1995/04/09 10:29:58;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

HEAD FOR THE HILLS -- This is a huge change.  Placements coming later.
Main pipe FC was updated too late on branches to be used on trgt ITag mtch.
  Tests tlb_1 and probably any unix notice.
Main pipe FL was updated too late on branches to be used on trgt ITag mtch.
  Even worse, it was way too late for ITLB to check br adrs on behalf of trgt.
  Found by inspection, maybe icache_except might notice.
rg/rgpc.V rg/rg.V euterpe.V:
  Delete pcr3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:

```

```

Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
icc/icc.V icc/icc_control.pim euterpe.V:
Add 5 stage shift register & snapper so ICC can capture a gva[63:48] on
branches and thus no longer need to continous ltlb of its own and so it
can get high gva in time for use on target.
icc/icc.V icc/icc_control.pim: Pipe for plR4 was 1 stage too short causing
cylinders to use others' priv levels. Probably is mostly responsible for
test icache except failure, but see bsrc/euterpe.status for another PL bug.
ife/ife.V ife/ifpcselil.Veqn: Merge ifp sel & ciRdNdx muxes in I2 stage
by getting rid of tag index mux fanin on ciRdNdx.
ife/ife.V ife/ifpcselil.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe
and snapped miss gva [47:12] to ICC so all in uniform place and to cut
control back & forth.
ife/ife.V: Detect mispredict recovery to sequential new
page & request corresponding hiccup to check protection. Found by inspection;
sinister protection implications if were not found.
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg???.pim:
Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
Delete pc[63:48] sent to for ICC's version of ltlb translation.
Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.
at/atpaselgen8.Veqn (delete) at/atpaselgen8.V (add) at/Makefile:
Reimplement so that gva input can be halfswing to handle new run to ICC.
at/at.V: Reorder dor pins into UfrcEnblR10 to be less X sensitive.
Rearrange hardware ifetch access physical address forcing to not force
gvaR8R9 input fullswing so can be halfswing to handle new run to ICC.
tst/spy.V: Eta spys were counting in wrong direction.
cj/Makefile: Add rsrvdedepi.tst rule.
yy/tas.pl: Deposit/withdraw & copyswap had obsolete opcode-number assignments.
{ife,cj,tst}/*rst.tst tst/drvchk.V: update to match other recent changes.
ife/iffree.tst: Earlier new reset PC experiments had broken.

```

```

-----
revision 87.1
date: 1995/04/09 10:29:51; author: mws; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/lt.V,v
Working file: verilog/bsrc/lt/lt.V
head: 3.72
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 72; selected revisions: 2
description:

```

```

-----
revision 3.71
date: 1995/04/12 04:06:16; author: woody; state: Exp; lines: +5 -2
Added flop in snkReq path. This allows the signal from GT to be half-swing and
should fixe the timing problem.

```

```

-----
revision 3.70
date: 1995/04/09 09:46:22; author: mws; state: Exp; lines: +73 -65
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg???.pim:

```

Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
Delete pc[63:48] sent to for ICC's version of ltlb translation.
Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/lt.power.tab.top,v
Working file: verilog/bsrc/lt/lt.power.tab.top
head: 68.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12; selected revisions: 1
description:

revision 68.10
date: 1995/04/10 20:01:08; author: chip; state: Exp; lines: +143 -147
new top-level io powerfile

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/lt_control.pim,v
Working file: verilog/bsrc/lt/lt_control.pim
head: 56.19
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 19; selected revisions: 3
description:

revision 56.16
date: 1995/04/12 04:06:19; author: woody; state: Exp; lines: +2 -1
Added flop in snkReq path. This allows the signal from GT to be half-swing and
should fix the timing problem.

revision 56.15
date: 1995/04/10 23:42:58; author: mws; state: Exp; lines: +85 -76
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg???.pim:
Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
Delete pc[63:48] sent to for ICC's version of ltlb translation.
Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.

revision 56.14
date: 1995/04/09 09:46:24; author: mws; state: Exp; lines: +16 -16
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg???.pim:
Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
Delete pc[63:48] sent to for ICC's version of ltlb translation.
Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/BOM,v

```

Working file: verilog/bsrc/mc/BOM
head: 79.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 157;   selected revisions: 4
description:
releasebom adding BOM
-----
revision 68.0
date: 1995/04/13 07:00:58; author: dickson; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/mc

move mc to the rigth 12 rows
-----
revision 67.1
date: 1995/04/13 07:00:49; author: dickson; state: Exp; lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
-----
revision 67.0
date: 1995/04/10 19:46:22; author: dickson; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/mc

move mc to the right
-----
revision 66.1
date: 1995/04/10 19:46:16; author: dickson; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/clean-request,v
Working file: verilog/bsrc/mc/clean-request
head: 17.19
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 19;   selected revisions: 2
description:
-----
revision 17.16
date: 1995/04/13 06:59:32; author: dickson; state: Exp; lines: +2 -1
move mc to the right (at this point only three collisions with xlu)
-----
revision 17.15
date: 1995/04/10 19:45:36; author: dickson; state: Exp; lines: +2 -1
move mc to the right
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/genpim.pl,v
Working file: verilog/bsrc/mc/genpim.pl
head: 13.17
branch:
locks: strict
access list:
keyword substitution: kv

```

```

total revisions: 17;    selected revisions: 2
description:
-----
revision 13.14
date: 1995/04/13 06:59:35;  author: dickson;  state: Exp;  lines: +4 -4
move mc to the right (at this point only three collisions with xlu)
-----
revision 13.13
date: 1995/04/10 19:45:37;  author: dickson;  state: Exp;  lines: +2 -2
move mc to the right
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/mc.power.tab.top,v
Working file: verilog/bsrc/mc/mc.power.tab.top
head: 37.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
-----
revision 37.8
date: 1995/04/10 20:01:14;  author: chip;  state: Exp;  lines: +1059 -1359
new top-level io powerfile
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mst/BOM,v
Working file: verilog/bsrc/mst/BOM
head: 38.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 74;    selected revisions: 2
description:
releasebom adding BOM
-----
revision 36.0
date: 1995/04/13 23:45:34;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu:
  Update placement to latest version. Still bigger than geert wants. Using some
  of the 4 rows above the reg file.
  uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the
  4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx timng fix.

cp:
  disable an internal mapping of cerberus space to flash rom.
  this function is only allowed by an external master poking at location '0'
  location '0' and '1' boot from local rom.
  all others boot over cerberus to master at location '0'

```

might be others

revision 35.1

date: 1995/04/13 23:45:25; author: woody; state: Exp; lines: +2 -2

releasebom: File needs to be up-to-date to use commit -r

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mst/mst.power.tab.top,v

Working file: verilog/bsrc/mst/mst.power.tab.top

head: 23.9

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 9; selected revisions: 1

description:

revision 23.8

date: 1995/04/10 20:01:23; author: chip; state: Exp; lines: +351 -423

new top-level io powerfile

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/BOM,v

Working file: verilog/bsrc/nb/BOM

head: 130.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 261; selected revisions: 2

description:

releasebom adding BOM

revision 121.0

date: 1995/04/13 23:46:07; author: woody; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

uu:

Update placement to latest version. Still bigger than geert wants. Using some of the 4 rows above the reg file.

uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the 4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx timng fix.

cp:

disable an internal mapping of cerberus space to flash rom.

this function is only allowed by an external master poking at location '0'

location '0' and '1' boot from local rom.

all others boot over cerberus to master at location '0'

might be others

revision 120.1

date: 1995/04/13 23:45:58; author: woody; state: Exp; lines: +9 -8
releasebom: File needs to be up-to-date to use commit -r

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/Makefile,v
Working file: verilog/bsrc/nb/Makefile
head: 1.45
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 45; selected revisions: 1
description:

revision 1.44
date: 1995/04/12 20:03:47; author: billz; state: Exp; lines: +2 -2
NBwed change. NBwed is generated one cycle earlier.
Becomes NBwedX0 at top level.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/nb.V,v
Working file: verilog/bsrc/nb/nb.V
head: 1.79
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 79; selected revisions: 1
description:

revision 1.78
date: 1995/04/12 20:03:50; author: billz; state: Exp; lines: +6 -4
NBwed change. NBwed is generated one cycle earlier.
Becomes NBwedX0 at top level.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/nb.power.tab.top,v
Working file: verilog/bsrc/nb/nb.power.tab.top
head: 82.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12; selected revisions: 1
description:

revision 82.8
date: 1995/04/10 20:01:35; author: chip; state: Exp; lines: +1909 -2099
new top-level io powerfile

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/nb_mid.pim,v
Working file: verilog/bsrc/nb/nb_mid.pim
head: 88.16
branch:
locks: strict
access list:


```

keyword substitution: kv
total revisions: 16;    selected revisions: 1
description:
-----
revision 88.14
date: 1995/04/12 20:03:57;  author: billz;  state: Exp;  lines: +5 -3
NBwed change. NBwed is generated one cycle earlier.
Becomes NBwedX0 at top level.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/nbctrl.Veqn,v
Working file: verilog/bsrc/nb/nbctrl.Veqn
head: 31.22
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 22;    selected revisions: 1
description:
-----
revision 31.22
date: 1995/04/12 20:04:02;  author: billz;  state: Exp;  lines: +3 -6
NBwed change. NBwed is generated one cycle earlier.
Becomes NBwedX0 at top level.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/nbtester.V,v
Working file: verilog/bsrc/nb/nbtester.V
head: 1.52
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 52;    selected revisions: 1
description:
-----
revision 1.52
date: 1995/04/12 20:04:05;  author: billz;  state: Exp;  lines: +2 -2
NBwed change. NBwed is generated one cycle earlier.
Becomes NBwedX0 at top level.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/nbvd.pla,v
Working file: verilog/bsrc/nb/nbvd.pla
head: 8.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;    selected revisions: 1
description:
-----
revision 8.5
date: 1995/04/12 20:04:07;  author: billz;  state: Exp;  lines: +3 -3
NBwed change. NBwed is generated one cycle earlier.
Becomes NBwedX0 at top level.
=====

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/nbwed.Veqn,v
Working file: verilog/bsrc/nb/nbwed.Veqn
head: 120.1

branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1; selected revisions: 1
description:

revision 120.1
date: 1995/04/12 20:04:10; author: billz; state: Exp;
NBwed change. NBwed is generated one cycle earlier.
Becomes NBwedX0 at top level.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/BOM,v
Working file: verilog/bsrc/rg/BOM
head: 136.0

branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 297; selected revisions: 8
description:

revision 114.0
date: 1995/04/12 20:16:58; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

rg/rgpc.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:
Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.
ALL (almost all) TESTS WILL NEED TO BE RECOMPILED.
Placement is not affected.

revision 113.1
date: 1995/04/12 20:16:49; author: mws; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r

revision 113.0
date: 1995/04/12 03:26:45; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

rg/rgpc.V rg/rg.V rgxmit/rgxmit.V uu/uu.V euterpe.V \
rg/rg.pim rgxmit/rgxmit_control.pim:
Eliminate midpipe undo increment feature by moving predicted br inc
suppression controls backward in pipe. Saves muxff2_62 (a strip at
least 7 atoms wide 434 atoms total) and associated metal4.
uu/gen_mem.pl uu/uu_drive.V: Update reserved xlu instr tests to drive X's
in the register number fields when possible.
uu/uumic.tst: Add a predicted taken blinki case.
tst/job.tst: r[abc] and op[abc] &OpPreps done before \$RDst stuff ready.
cdio/cdio.V: Was copying the low datain to high datain for the 2nd half of
the CD write cycle.

revision 112.1

date: 1995/04/12 03:26:37; author: mws; state: Exp; lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r

revision 112.0

date: 1995/04/11 07:31:46; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

Noncrashing placements for rg, au (no change), rgxmit, lt, at.
This leaves just uu, ife, and icc yet to place.

revision 111.1

date: 1995/04/11 07:31:37; author: mws; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r

revision 111.0

date: 1995/04/09 10:31:02; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

HEAD FOR THE HILLS -- This is a huge change. Placements coming later.
Main pipe PC was updated too late on branches to be used on trgt ITag mtch.
Tests tlb 1 and probably any unix notice.
Main pipe PL was updated too late on branches to be used on trgt ITag mtch.
Even worse, it was way too late for LTLB to check br adrs on behalf of trgt.
Found by inspection, maybe icache_except might notice.
rg/rgpc.V rg/rg.V euterpe.V:
Delete pcr3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprbldmr5.Veqn uu/uuprbldmr7.Veqn uu/uu.V euterpe.V:
Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
icc/icc.V icc/icc.control.pim euterpe.V:
Add 5 stage shift register & snapper so ICC can capture a gva[63:48] on
branches and thus no longer need to continous ltlb of its own and so it
can get high gva in time for use on target.
icc/icc.V icc/icc.control.pim: Pipe for plR4 was 1 stage too short causing
cylinders to use others' priv levels. Probably is mostly responsible for
test icache_except failure, but see bsrc/euterpe.status for another PL bug.
ife/ife.V ife/ifpcselil.Veqn: Merge ifp sel & ciRdNdx muxes in I2 stage
by getting rid of tag index mux fanin on ciRdNdx.
ife/ife.V ife/ifpcselil.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe
and snapped miss gva [47:12] to ICC so all in uniform place and to cut
control back & forth.
ife/ife.V: Detect mispredict recovery to sequential new
page & request corresponding hiccup to check protection. Found by inspection;
sinister protection implications if were not found.
lt/lt.V lt.control.pim euterpe.V icc.V rg/rgpc.V rg/rg???.pim:
Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
Delete pc[63:48] sent to for ICC's version of ltlb translation.
Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.
at/atpaselgen8.Veqn (delete) at/atpaselgen8.V (add) at/Makefile:
Reimplement so that gva input can be halfswing to handle new run to ICC.
at/at.V: Reorder dor pins into UfrcEnblR10 to be less X sensitive.
Rearrange hardware ifetch access physical address forcing to not force
gvaR8R9 input fullswing so can be halfswing to handle new run to ICC.
tst/spy.V: Eta spys were counting in wrong direction.
cj/Makefile: Add rsrvdedepi.tst rule.
yy/tas.pl: Deposit/withdraw & copyswap had obsolete opcode-number assignments.
{ife,cj,tst}/*rst.tst tst/drvchk.V: update to match other recent changes.

```

ife/iffree.tst: Earlier new reset PC experiments had broken.
-----
revision 110.1
date: 1995/04/09 10:30:55; author: mws; state: Exp; lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rg.V,v
Working file: verilog/bsrc/rg/rg.V
head: 29.17
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 17; selected revisions: 2
description:
-----

```

```

revision 29.17
date: 1995/04/12 03:20:21; author: mws; state: Exp; lines: +1 -4
rg/rgpc.V rg/rg.V rgxmit/rgxmit.V uu/uu.V euterpe.V \
rg/rg.pim rgxmit/rgxmit_control.pim:
    Eliminate midpipe undo increment feature by moving predicted br inc
    suppression controls backward in pipe. Saves muxff2_62 (a strip at
    least 7 atoms wide 434 atoms total) and associated metal4.
-----

```

```

revision 29.16
date: 1995/04/09 09:47:34; author: mws; state: Exp; lines: +35 -37
rg/rgpc.V rg/rg.V euterpe.V:
    Delete pcR3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg???.pim:
    Delete lt1b xor data formerly sent to ICC so that it could do own xlation.
    Delete pc[63:48] sent to for ICC's version of lt1b translation.
    Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rg.pim,v
Working file: verilog/bsrc/rg/rg.pim
head: 82.31
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 31; selected revisions: 2
description:
-----

```

```

revision 82.18
date: 1995/04/12 03:20:24; author: mws; state: Exp; lines: +404 -404
rg/rgpc.V rg/rg.V rgxmit/rgxmit.V uu/uu.V euterpe.V \
rg/rg.pim rgxmit/rgxmit_control.pim:
    Eliminate midpipe undo increment feature by moving predicted br inc
    suppression controls backward in pipe. Saves muxff2_62 (a strip at
    least 7 atoms wide 434 atoms total) and associated metal4.
-----

```

```

revision 82.17
date: 1995/04/10 22:11:44; author: mws; state: Exp; lines: +76 -74
rg/rgpc.V rg/rg.V euterpe.V:

```

```

Delete pcr3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcpth.
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg???.pim:
Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
Delete pc[63:48] sent to for ICC's version of ltlb translation.
Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rg.power.tab.top,v
Working file: verilog/bsrc/rg/rg.power.tab.top
head: 79.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
-----
revision 79.8
date: 1995/04/10 20:01:47;  author: chip;  state: Exp;  lines: +583 -587
new top-level io powerfile
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rgpc.V,v
Working file: verilog/bsrc/rg/rgpc.V
head: 1.33
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 33;    selected revisions: 3
description:
PC (program counter) address path.
Intended to go in the main data path with rgdp.V.
-----
revision 1.31
date: 1995/04/12 20:03:53;  author: mws;  state: Exp;  lines: +10 -10
rg/rgpc.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:
Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.
-----

```

```

revision 1.30
date: 1995/04/12 03:20:26;  author: mws;  state: Exp;  lines: +14 -26
rg/rgpc.V rg/rg.V rgxmit/rgxmit.V uu/uu.V euterpe.V \
rg/rg.pim rgxmit/rgxmit_control.pim:
Eliminate midpipe undo increment feature by moving predicted br inc
suppression controls backward in pipe. Saves muxff2_62 (a strip at
least 7 atoms wide 434 atoms total) and associated metal4.
-----

```

```

revision 1.29
date: 1995/04/09 09:47:36;  author: mws;  state: Exp;  lines: +44 -38
rg/rgpc.V rg/rg.V euterpe.V:
Delete pcr3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg???.pim:
Delete ltlb xor data formerly sent to ICC so that it could do own xlation.

```

Delete pc[63:48] sent to for ICC's version of ltlb translation.
Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rgplr0.pla,v
Working file: verilog/bsrc/rg/rgplr0.pla
head: 52.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2; selected revisions: 1
description:

revision 52.2
date: 1995/04/09 09:47:38; author: mws; state: Exp; lines: +17 -17
rg/rgpc.V rg/rg.V euterpe.V:
Delete pcr3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg??pim:
Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
Delete pc[63:48] sent to for ICC's version of ltlb translation.
Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rgrst.tst,v
Working file: verilog/bsrc/rg/rgrst.tst
head: 9.28
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 28; selected revisions: 1
description:

revision 9.25
date: 1995/04/09 09:47:39; author: mws; state: Exp; lines: +2 -2
rg/rgpc.V rg/rg.V euterpe.V:
Delete pcr3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg??pim:
Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
Delete pc[63:48] sent to for ICC's version of ltlb translation.
Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rgxmit/BOM,v
Working file: verilog/bsrc/rgxmit/BOM
head: 42.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 82; selected revisions: 6
description:
releasebom adding BOM

```

revision 40.0
date: 1995/04/12 03:27:08; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

rg/rgpc.V rg/rg.V rgxmit/rgxmit.V uu/uu.V euterpe.V \
rg/rg.pim rgxmit/rgxmit_control.pim:
    Eliminate midpipe undo increment feature by moving predicted br inc
    suppression controls backward in pipe. Saves muxff2_62 (a strip at
    least 7 atoms wide 434 atoms total) and associated metal4.
uu/gen mem.pl uu/uu_drive.V: Update reserved xlu instr tests to drive X's
    in the register number fields when possible.
uu/uumic.tst: Add a predicted taken blinki case.
tst/job.tst: r[abc] and op[abc] &OpPreps done before $RDst stuff ready.
cdio/cdio.V: Was copying the low datain to high datain for the 2nd half of
    the CD write cycle.

```

```

-----
revision 39.1
date: 1995/04/12 03:27:01; author: mws; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r

```

```

-----
revision 39.0
date: 1995/04/11 07:41:55; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

```

Noncrashing placements for rg, au (no change), rgxmit, lt, at.
This leaves just uu, ife, and icc yet to place.
Also grab new veena reserved instr tests in uu.

```

-----
revision 38.1
date: 1995/04/11 07:41:48; author: mws; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r

```

```

-----
revision 38.0
date: 1995/04/09 10:31:23; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

```

HEAD FOR THE HILLS -- This is a huge change. Placements coming later.
Main pipe FC was updated too late on branches to be used on trgt ITag mtch.
Tests tlb 1 and probably any unix notice.
Main pipe PL was updated too late on branches to be used on trgt ITag mtch.
Even worse, it was way too late for LTLB to check br adrs on behalf of trgt.
Found by inspection, maybe icache_except might notice.

```

rg/rgpc.V rg/rg.V euterpe.V:
    Delete pcr3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
    Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
icc/icc.V icc/icc_control.pim euterpe.V:
    Add 5 stage shift register & snapper so ICC can capture a gva[63:48] on
    branches and thus no longer need to continous ltlb of its own and so it
    can get high gva in time for use on target.
icc/icc.V icc/icc_control.pim: Pipe for plR4 was 1 stage too short causing
    cylinders to use others' priv levels. Probably is mostly responsible for
    test icache_except failure, but see bsrc/euterpe.status for another PL bug.
ife/ife.V ife/ifpcsel11.Veqn: Merge ifp sel & ciRdNdx muxes in I2 stage
    by getting rid of tag index mux fanin on ciRdNdx.
ife/ife.V ife/ifpcsel11.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe

```

```

and snapped miss gva [47:12] to ICC so all in uniform place and to cut
control back & forth.
ife/ife.V: Detect mispredict recovery to sequential new
page & request corresponding hiccup to check protection. Found by inspection;
sinister protection implications if were not found.
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg??pim:
Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
Delete pc[63:48] sent to for ICC's version of ltlb translation.
Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.
at/atpaselgen8.Veqn (delete) at/atpaselgen8.V (add) at/Makefile:
Reimplement so that gva input can be halfswing to handle new run to ICC.
at/at.V: Reorder dor pins into UfrcEnblR10 to be less X sensitive.
Rearrange hardware ifetch access physical address forcing to not force
gvaR8R9 input fullswing so can be halfswing to handle new run to ICC.
tst/spy.V: Eta spys were counting in wrong direction.
cj/Makefile: Add rsrvdedep1.tst rule.
yy/tas.pl: Deposit/withdraw & copyswap had obsolete opcode-number assignments.
{ife,cj,tst}/*rst.tst tst/drvchk.V: update to match other recent changes.
ife/iffree.tst: Earlier new reset PC experiments had broken.

```

```

-----
revision 37.1
date: 1995/04/09 10:31:16; author: mws; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rgxmit/rgxmit.V,v
Working file: verilog/bsrc/rgxmit/rgxmit.V
head: 1.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 24; selected revisions: 2
description:
-----

```

```

revision 1.24
date: 1995/04/12 03:11:31; author: mws; state: Exp; lines: +22 -23
rg/rgpc.V rg/rg.V rgxmit/rgxmit.V uu/uu.V euterpe.V \
rg/rg.pim rgxmit/rgxmit_control.pim:
Eliminate midpipe undo increment feature by moving predicted br inc
suppression controls backward in pipe. Saves muxff2_62 (a strip at
least 7 atoms wide 434 atoms total) and associated metal4.
-----
revision 1.23
date: 1995/04/09 09:48:07; author: mws; state: Exp; lines: +10 -12
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rgxmit/rgxmit.power.tab.top,v
Working file: verilog/bsrc/rgxmit/rgxmit.power.tab.top
head: 19.6
branch:
locks: strict
access list:
keyword substitution: kv

```



```

total revisions: 6;      selected revisions: 1
description:
-----
revision 19.5
date: 1995/04/10 20:01:52;  author: chip;  state: Exp;  lines: +49 -69
new top-level io powerfile
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rgxmit/rgxmit_control.pim,v
Working file: verilog/bsrc/rgxmit/rgxmit_control.pim
head: 1.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16;      selected revisions: 2
description:
-----
revision 1.15
date: 1995/04/12 03:11:33;  author: mws;  state: Exp;  lines: +4 -4
rg/rgpc.V rg/rg.V rgxmit/rgxmit.V uu/uu.V euterpe.V \
rg/rg.pim rgxmit/rgxmit_control.pim:
    Eliminate midpipe undo increment feature by moving predicted br inc
    suppression controls backward in pipe.  Saves muxff2_62 (a strip at
    least 7 atoms wide 434 atoms total) and associated metal4.
-----
revision 1.14
date: 1995/04/10 22:30:26;  author: mws;  state: Exp;  lines: +8 -5
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
    Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/BOM,v
Working file: verilog/bsrc/sr/BOM
head: 75.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 148;      selected revisions: 2
description:
releasebom adding BOM
-----
revision 61.0
date: 1995/04/13 23:47:01;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu:
    Update placement to latest version.  Still bigger than geert wants.  Using some
    of the 4 rows above the reg file.
    uu-local-p4.obs is used when doing a mincut.  This obs leaves some space in the
    4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx timng fix.

```

```
cp:
  disable an internal mapping of cerberus space to flash rom.
  this function is only allowed by an external master poking at location '0'
  location '0' and '1' boot from local rom.
  all others boot over cerberus to master at location '0'
```

might be others

```
-----
revision 60.1
date: 1995/04/13 23:46:54; author: woody; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/genpim.pl,v
Working file: verilog/bsrc/sr/genpim.pl
head: 16.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14; selected revisions: 1
description:
-----
```

```
revision 16.13
date: 1995/04/11 21:02:02; author: chip; state: Exp; lines: +2 -2
Moved orif gin a bit to the left
```

Geert

```
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/sr.power.tab.top,v
Working file: verilog/bsrc/sr/sr.power.tab.top
head: 39.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10; selected revisions: 1
description:
-----
```

```
revision 39.8
date: 1995/04/10 20:01:56; author: chip; state: Exp; lines: +1218 -1068
new top-level io powerfile
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/BOM,v
Working file: verilog/bsrc/tst/BOM
head: 112.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 234; selected revisions: 6
description:
releasebom adding BOM
-----
```

```

revision 105.0
date: 1995/04/12 20:17:43; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

rg/rgpc.V tst/rst.tst ife/*.tst cj/*.tst uu/(br,uumic).tst euterpe.status:
  Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.
  ALL (almost all) TESTS WILL NEED TO BE RECOMPILED.
  Placement is not affected.
-----
revision 104.1
date: 1995/04/12 20:17:34; author: mws; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
-----
revision 104.0
date: 1995/04/12 03:27:43; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

rg/rgpc.V rg/rg.V rgxmit/rgxmit.V uu/uu.V euterpe.V \
rg/rg.pim rgxmit/rgxmit_control.pim:
  Eliminate midpipe undo increment feature by moving predicted br inc
  suppression controls backward in pipe. Saves muxff2_62 (a strip at
  least 7 atoms wide 434 atoms total) and associated metal4.
uu/gen_mem.pl uu/uu_drive.V: Update reserved xlu instr tests to drive X's
  in the register number fields when possible.
uu/uumic.tst: Add a predicted taken blinki case.
tst/job.tst: r[abc] and op[abc] &OpPreps done before $RDst stuff ready.
cdio/cdio.V: Was copying the low datain to high datain for the 2nd half of
  the CD write cycle.
-----
revision 103.1
date: 1995/04/12 03:27:36; author: mws; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
-----
revision 103.0
date: 1995/04/09 10:31:50; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

HEAD FOR THE HILLS -- This is a huge change. Placements coming later.
Main pipe PC was updated too late on branches to be used on trgt ITag mtch.
  Tests tlb_1 and probably any unix notice.
Main pipe PL was updated too late on branches to be used on trgt ITag mtch.
  Even worse, it was way too late for LTLB to check br adrs on behalf of trgt.
  Found by inspection, maybe icache_except might notice.
rg/rgpc.V rg/rg.V euterpe.V:
  Delete pcr3R4[63:48] pCbffrd[46:15] now that ICC gets from GT.
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
  Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
icc/icc.V icc/icc_control.pim euterpe.V:
  Add 5 stage shift register & snapper so ICC can capture a gva[63:48] on
  branches and thus no longer need to continous ltlb of its own and so it
  can get high gva in time for use on target.
icc/icc.V icc/icc_control.pim: Pipe for plR4 was 1 stage too short causing
  cylinders to use others' priv levels. Probably is mostly responsible for
  test icache_except failure, but see bsrc/euterpe.status for another PL bug.
ife/ife.V ife/ifpcsel11.Veqn: Merge ifp sel & ciRdNdx muxes in I2 stage
  by getting rid of tag index mux fanin on ciRdNdx.

```

```

ife/ife.V ife/ifpcselil.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe
and snapped miss gva [47:12] to ICC so all in uniform place and to cut
control back & forth.
ife/ife.V: Detect mispredict recovery to sequential new
page & request corresponding hiccup to check protection. Found by inspection;
sinister protection implications if were not found.
lt/lt.V lt_control.pim euterpe.V icc.V rg/rgpc.V rg/rg??pim:
Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
Delete pc[63:48] sent to for ICC's version of ltlb translation.
Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.
at/atpaselgen8.Veqn (delete) at/atpaselgen8.V (add) at/Makefile:
Reimplement so that gva input can be halfswing to handle new run to ICC.
at/at.V: Reorder dor pins into UfrcEnblR10 to be less X sensitive.
Rearrange hardware ifetch access physical address forcing to not force
gvaR8R9 input fullswing so can be halfswing to handle new run to ICC.
tst/spy.V: Eta spys were counting in wrong direction.
cj/Makefile: Add rsrvdedepi.tst rule.
yy/tas.pl: Deposit/withdraw & copyswap had obsolete opcode-number assignments.
{ife,cj,tst}/*rst.tst tst/drvchk.V: update to match other recent changes.
ife/iffree.tst: Earlier new reset PC experiments had broken.

```

```

-----
revision 102.1

```

```

date: 1995/04/09 10:31:43; author: mws; state: Exp; lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r

```

```

=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/drvchk.V,v

```

```

Working file: verilog/bsrc/tst/drvchk.V

```

```

head: 1.85

```

```

branch:

```

```

locks: strict

```

```

access list:

```

```

keyword substitution: kv

```

```

total revisions: 85; selected revisions: 2

```

```

description:

```

```

-----
revision 1.79

```

```

date: 1995/04/14 05:29:24; author: woody; state: Exp; lines: +3 -3
Change interface name NBweDX1 to NBweDX0.

```

```

-----
revision 1.78

```

```

date: 1995/04/09 09:54:48; author: mws; state: Exp; lines: +11 -6

```

```

Main pipe PC was updated too late on branches to be used on trgt ITag mtch.

```

```

Tests tlb_1 and probably any unix notice.

```

```

Main pipe PL was updated too late on branches to be used on trgt ITag mtch.

```

```

Even worse, it was way too late for LTLB to check br adrs on behalf of trgt.

```

```

Found by inspection, maybe icache_except might notice.

```

```

tst/spy.V: Eta spys were counting in wrong direction.

```

```

=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/job.tst,v

```

```

Working file: verilog/bsrc/tst/job.tst

```

```

head: 6.41

```

```

branch:

```

```

locks: strict

```

```

access list:

```

```

keyword substitution: kv

```

```

total revisions: 41;    selected revisions: 1
description:
-----
revision 6.37
date: 1995/04/12 03:16:58; author: mws; state: Exp; lines: +9 -8
tst/job.tst:  r[abc] and op[abc] &OpPreps done before $RDst stuff ready.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/rst.tst,v
Working file: verilog/bsrc/tst/rst.tst
head: 1.30
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 30;    selected revisions: 1
description:
-----
revision 1.29
date: 1995/04/12 20:03:24; author: mws; state: Exp; lines: +3 -3
rg/rqpc.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:
Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/spy.V,v
Working file: verilog/bsrc/tst/spy.V
head: 1.17
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 17;    selected revisions: 1
description:
-----
revision 1.17
date: 1995/04/09 09:54:49; author: mws; state: Exp; lines: +13 -12
Main pipe PC was updated too late on branches to be used on trgt ITag mtch.
Tests tlb_1 and probably any unix notice.
Main pipe PL was updated too late on branches to be used on trgt ITag mtch.
Even worse, it was way too late for LTLB to check br adrs on behalf of trgt.
Found by inspection, maybe icache except might notice.
tst/spy.V: Eta spys were counting in wrong direction.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/tstrst.tst,v
Working file: verilog/bsrc/tst/tstrst.tst
head: 6.35
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 35;    selected revisions: 1
description:
-----
revision 6.32
date: 1995/04/09 09:54:51; author: mws; state: Exp; lines: +3 -3
Main pipe PC was updated too late on branches to be used on trgt ITag mtch.

```

Tests tlb_1 and probably any unix notice.
Main pipe PL was updated too late on branches to be used on trgt ITag mch.
Even worse, it was way too late for ITLB to check br adrs on behalf of trgt.
Found by inspection, maybe icache except might notice.
tst/spy.V: Eta spys were counting in wrong direction.

```
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/.checkoutrc,v
Working file: verilog/bsrc/uu/.checkoutrc
head: 79.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;    selected revisions: 1
description:
-----
revision 79.3
date: 1995/04/12 21:40:35;  author: woody;  state: Exp;  lines: +2 -2
Change GARDS_DISPLAY to hard038.
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/BOM,v
Working file: verilog/bsrc/uu/BOM
head: 218.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 480;    selected revisions: 12
description:
-----
revision 181.0
date: 1995/04/13 23:47:43;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc
```

uu:
Update placement to latest version. Still bigger than geert wants. Using some
of the 4 rows above the reg file.
uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the
4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx timng fix.

cp:
disable an internal mapping of cerberus space to flash rom.
this function is only allowed by an external master poking at location '0'
location '0' and '1' boot from local rom.
all others boot over cerberus to master at location '0'

might be others

```
-----
revision 180.1
date: 1995/04/13 23:47:34;  author: woody;  state: Exp;  lines: +6 -5
releasebom: File needs to be up-to-date to use commit -r
```

revision 180.0

date: 1995/04/12 20:18:20; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

rg/rgpc.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:

Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.

ALL (almost all) TESTS WILL NEED TO BE RECOMPILED.

Placement is not affected.

revision 179.1

date: 1995/04/12 20:18:11; author: mws; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r

revision 179.0

date: 1995/04/12 03:28:16; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

rg/rgpc.V rg/rg.V rgxmit/rgxmit.V uu/uu.V euterpe.V \
rg/rg.pim rgxmit/rgxmit_control.pim:

Eliminate midpipe undo increment feature by moving predicted br inc
suppression controls backward in pipe. Saves muxff2_62 (a strip at
least 7 atoms wide 434 atoms total) and associated metal4.

uu/gen_mem.pl uu/uu_drive.V: Update reserved xlu instr tests to drive X's
in the register number fields when possible.

uu/uumic.tst: Add a predicted taken blinki case.

tst/job.tst: r[abc] and op[abc] &OpPreps done before \$RDst stuff ready.

cdio/cdio.V: Was copying the low datain to high datain for the 2nd half of
the CD write cycle.

revision 178.1

date: 1995/04/12 03:28:08; author: mws; state: Exp; lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r

revision 178.0

date: 1995/04/11 07:42:35; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

Noncrashing placements for rg, au (no change), rgxmit, lt, at.

This leaves just uu, ife, and icc yet to place.

Also grab new veena reserved instr tests in uu.

revision 177.1

date: 1995/04/11 07:42:27; author: mws; state: Exp; lines: +4 -1
releasebom: File needs to be up-to-date to use commit -r

revision 177.0

date: 1995/04/11 07:32:52; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

Noncrashing placements for rg, au (no change), rgxmit, lt, at.

This leaves just uu, ife, and icc yet to place.

revision 176.1

date: 1995/04/11 07:32:38; author: mws; state: Exp; lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r

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revision 176.0
date: 1995/04/09 10:32:18; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

HEAD FOR THE HILLS -- This is a huge change. Placements coming later.
Main pipe PC was updated too late on branches to be used on trgt ITag mtch.
Tests tl1b 1 and probably any unix notice.
Main pipe PL was updated too late on branches to be used on trgt ITag mtch.
Even worse, it was way too late for LTLB to check br adrs on behalf of trgt.
Found by inspection, maybe icache_except might notice.
rg/rgpc.V rg/rg.V euterpe.V:
Delete pcr3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
icc/icc.V icc/icc.control.pim euterpe.V:
Add 5 stage shift register & snapper so ICC can capture a gva[63:48] on
branches and thus no longer need to continous ltlb of its own and so it
can get high gva in time for use on target.
icc/icc.V icc/icc.control.pim: Pipe for plR4 was 1 stage too short causing
cylinders to use others' priv levels. Probably is mostly responsible for
test icache_except failure, but see bsrc/euterpe.status for another PL bug.
ife/ife.V ife/ifpcsel1l.Veqn: Merge ifp sel & ciRdNdx muxes in I2 stage
by getting rid of tag index mux fanin on ciRdNdx.
ife/ife.V ife/ifpcsel1l.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe
and snapped miss gva [47:12] to ICC so all in uniform place and to cut
control back & forth.
ife/ife.V: Detect mispredict recovery to sequential new
page & request corresponding hiccup to check protection. Found by inspection;
sinister protection implications if were not found.
lt/lt.V lt.control.pim euterpe.V icc.V rg/rgpc.V rg/rg??pim:
Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
Delete pc[63:48] sent to for ICC's version of ltlb translation.
Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.
at/atpaselgen8.Veqn (delete) at/atpaselgen8.V (add) at/Makefile:
Reimplement so that gva input can be halfswing to handle new run to ICC.
at/at.V: Reorder dor pins into UfrcEnblR10 to be less X sensitive.
Rearrange hardware ifetch access physical address forcing to not force
gvaR8R9 input fullswing so can be halfswing to handle new run to ICC.
tst/spy.V: Eta spys were counting in wrong direction.
cj/Makefile: Add rsrvdedepi.tst rule.
yy/tas.pl: Deposit/withdraw & copyswap had obsolete opcode-number assignments.
{ife,cj,tst}/*rst.tst tst/drvchk.V: update to match other recent changes.
ife/iffree.tst: Earlier new reset PC experiments had broken.
-----

```

```

revision 175.1
date: 1995/04/09 10:32:11; author: mws; state: Exp; lines: +10 -10
releasebom: File needs to be up-to-date to use commit -r
-----

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/br.tst,v
Working file: verilog/bsrc/uu/br.tst
head: 2.14
branch:
locks: strict
access list:
keyword substitution: kv

```



```

total revisions: 14;    selected revisions: 1
description:
-----
revision 2.14
date: 1995/04/12 20:01:48; author: mws; state: Exp; lines: +18 -19
rg/rGPC.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:
  Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/evblm.prio,v
Working file: verilog/bsrc/uu/evblm.prio
head: 131.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;    selected revisions: 1
description:
-----
revision 131.8
date: 1995/04/09 09:51:18; author: mws; state: Exp; lines: +3 -3
rg/rGPC.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
  Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/gen_mem.pl,v
Working file: verilog/bsrc/uu/gen_mem.pl
head: 174.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;    selected revisions: 1
description:
-----
revision 174.2
date: 1995/04/12 01:52:20; author: veena; state: Exp; lines: +206 -66
changed uu instantiation to match the interface changes. uu_drive now reads
binary file instead of hex so x's can be put for register numbers. (X is used
in all but lsb for g-ops which need register-pairs, X is used in bits for e-ops
that don't require pairs. Simulation passes all XLU exception-cases.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/genpim.pl,v
Working file: verilog/bsrc/uu/genpim.pl
head: 68.17
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 17;    selected revisions: 1
description:
-----
revision 68.15
date: 1995/04/13 23:32:50; author: woody; state: Exp; lines: +5 -3
Update placement to latest version. Still bigger than geert wants. Using some

```

of the 4 rows above the reg file.
uu-local-p4.obs should be used when doing a mincut. This obs leaves some space
in the 4 rows for powering up without running in to ES.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu-local-p4.obs,v

Working file: verilog/bsrc/uu/uu-local-p4.obs

head: 180.1

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 1; selected revisions: 1

description:

revision 180.1

date: 1995/04/13 23:32:53; author: woody; state: Exp;

Update placement to latest version. Still bigger than geert wants. Using some
of the 4 rows above the reg file.

uu-local-p4.obs should be used when doing a mincut. This obs leaves some space
in the 4 rows for powering up without running in to ES.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu-local.obs,v

Working file: verilog/bsrc/uu/uu-local.obs

head: 123.4

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 4; selected revisions: 1

description:

revision 123.4

date: 1995/04/10 23:46:38; author: woody; state: Exp; lines: +1 -1

add in the rows over the reg file.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu.V,v

Working file: verilog/bsrc/uu/uu.V

head: 1.202

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 202; selected revisions: 5

description:

issue unit

revision 1.177

date: 1995/04/13 23:32:56; author: woody; state: Exp; lines: +9 -9

Update placement to latest version. Still bigger than geert wants. Using some
of the 4 rows above the reg file.

uu-local-p4.obs should be used when doing a mincut. This obs leaves some space
in the 4 rows for powering up without running in to ES.

revision 1.176

- .

date: 1995/04/12 20:06:43; author: billz; state: Exp; lines: +5 -3
NBwed change. NBwed is generated one cycle earlier.
Becomes NBwedX0 at top level.

Note, within uu, have added instance of ff_1, UnbWeDX1.
Have not updated placement, but obviously this
should be next to UnbWeDX2.

The interface to uu has changed, in that,
UnbWeDX0 replaces UnbWeDX1.

revision 1.175

date: 1995/04/12 03:13:49; author: mws; state: Exp; lines: +13 -4
rg/rgpc.V rg/rg.V rgxmit/rgxmit.V uu/uu.V euterpe.V \
rg/rg.pim rgxmit/rgxmit_control.pim:
Eliminate midpipe undo increment feature by moving predicted br inc
suppression controls backward in pipe. Saves muxff2_62 (a strip at
least 7 atoms wide 434 atoms total) and associated metal4.
uu/uumic.tst: Add a predicted taken blink1 case.

revision 1.174

date: 1995/04/09 11:14:53; author: mws; state: Exp; lines: +142 -3
Add scalar wire declarations.

revision 1.173

date: 1995/04/09 09:51:22; author: mws; state: Exp; lines: +31 -187
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcpth.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu.power.tab.top,v

Working file: verilog/bsrc/uu/uu.power.tab.top

head: 119.13

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 13; selected revisions: 1

description:

revision 119.6

date: 1995/04/10 20:02:03; author: chip; state: Exp; lines: +2649 -2223

new top-level io powerfile

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu_control.pim,v

Working file: verilog/bsrc/uu/uu_control.pim

head: 68.60

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 60; selected revisions: 1

description:

revision 68.38

date: 1995/04/13 23:33:09; author: woody; state: Exp; lines: +4671 -5835
Update placement to latest version. Still bigger than geert wants. Using some
of the 4 rows above the reg file.
uu-local-p4.obs should be used when doing a mincut. This obs leaves some space
in the 4 rows for powering up without running in to ES.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu_drive.V,v
Working file: verilog/bsrc/uu/uu_drive.V
head: 174.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3; selected revisions: 1
description:

revision 174.2
date: 1995/04/12 01:52:17; author: veena; state: Exp; lines: +8 -9
changed uu instantiation to match the interface changes. uu_drive now reads
binary file instead of hex so x's can be put for register numbers. (X is used
in all but lsb for g-ops which need register-pairs, X is used in bits for e-ops
that don't require pairs. Simulation passes all XLU exception-cases.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uumic.tst,v
Working file: verilog/bsrc/uu/uumic.tst
head: 8.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15; selected revisions: 2
description:

revision 8.15
date: 1995/04/12 20:01:50; author: mws; state: Exp; lines: +2 -3
rg/rgpc.V tst/rst.tst ife/*.tst cj/*.tst uu/{br,uumic}.tst euterpe.status:
Change reset PC from 0000_4000_0000_0000 to 0000_4000_0000_0200.

revision 8.14
date: 1995/04/12 03:13:52; author: mws; state: Exp; lines: +22 -3
rg/rgpc.V rg/rg.V rgxmit/rgxmit.V uu/uu.V euterpe.V \
rg/rg.pim rgxmit/rgxmit_control.pim:
Eliminate midpipe undo increment feature by moving predicted br inc
suppression controls backward in pipe. Saves muxff2_62 (a strip at
least 7 atoms wide 434 atoms total) and associated metal4.
uu/uumic.tst: Add a predicted taken blinki case.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uuprblmr5.Veqn,v
Working file: verilog/bsrc/uu/uuprblmr5.Veqn
head: 50.11
branch:
locks: strict
access list:
keyword substitution: kv

```

total revisions: 11;    selected revisions: 1
description:
-----
revision 50.11
date: 1995/04/09 09:51:26; author: mws; state: Exp; lines: +19 -53
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
    Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uuprblmr7.Veqn,v
Working file: verilog/bsrc/uu/uuprblmr7.Veqn
head: 107.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
-----
revision 107.11
date: 1995/04/09 09:51:27; author: mws; state: Exp; lines: +34 -5
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
    Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uurst.tst,v
Working file: verilog/bsrc/uu/uurst.tst
head: 15.30
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 30;    selected revisions: 2
description:
-----
revision 15.28
date: 1995/04/14 05:28:48; author: woody; state: Exp; lines: +2 -2
Change interface name NBweDX1 to NBweDX0.
=====
revision 15.27
date: 1995/04/09 09:51:28; author: mws; state: Exp; lines: +2 -2
rg/rgpc.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprblmr5.Veqn uu/uuprblmr7.Veqn uu/uu.V euterpe.V:
    Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/xlu/BOM,v
Working file: verilog/bsrc/xlu/BOM
head: 65.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 132;    selected revisions: 2
description:

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```

releasebom adding BOM
-----
revision 53.0
date: 1995/04/13 23:48:09; author: woody; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu:
  Update placement to latest version. Still bigger than geert wants. Using some
  of the 4 rows above the reg file.
  uu-local-p4.obs is used when doing a mincut. This obs leaves some space in the
  4 rows for powering up without running in to ES.

nb,uu, euterpe.V: nbWeDX1 timing fix.

au: auindx timng fix.

cp:
  disable an internal mapping of cerberus space to flash rom.
  this function is only allowed by an external master poking at location '0'
  location '0' and '1' boot from local rom.
  all others boot over cerberus to master at location '0'

might be others
-----
revision 52.1
date: 1995/04/13 23:48:01; author: woody; state: Exp; lines: +2 -3
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/xlu/xlu.power.tab.top,v
Working file: verilog/bsrc/xlu/xlu.power.tab.top
head: 48.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;      selected revisions: 1
description:
-----
revision 48.3
date: 1995/04/10 20:02:12; author: chip; state: Exp; lines: +729 -729
new top-level io powerfile
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/yy/BOM,v
Working file: verilog/bsrc/yy/BOM
head: 26.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 61;      selected revisions: 2
description:
-----
revision 26.0
date: 1995/04/09 10:32:48; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

```

```

HEAD FOR THE HILLS -- This is a huge change.  Placements coming later.
Main pipe PC was updated too late on branches to be used on trgt ITag mtch.
  Tests tlbl_1 and probably any unix notice.
Main pipe PL was updated too late on branches to be used on trgt ITag mtch.
  Even worse, it was way too late for LTLB to check br adrs on behalf of trgt.
  Found by inspection, maybe icache_except might notice.
rg/rGPC.V rg/rg.V euterpe.V:
  Delete pcr3R4[63:48] pcBffrd[46:15] now that ICC gets from GT.
rg/rGPC.V rg/rg.V au/auindx.V rgxmit/rgxmit.V lt/lt.V at/at.V \
icc/icc.V uu/evblm.prio uu/uuprbmlr5.Veqn uu/uuprbmlr7.Veqn uu/uu.V euterpe.V:
  Move priv level pipe updates 8 ticks sooner so br's can see PL for trgt xcptn.
icc/icc.V icc/icc.control.pim euterpe.V:
  Add 5 stage shift register & snapper so ICC can capture a gva[63:48] on
  branches and thus no longer need to continous ltlb of its own and so it
  can get high gva in time for use on target.
icc/icc.V icc/icc.control.pim: Pipe for plR4 was 1 stage too short causing
  cylinders to use others' priv levels.  Probably is mostly responsible for
  test icache_except failure, but see bsrc/euterpe.status for another PL bug.
ife/ife.V ife/ifpcselil.Veqn: Merge ifp sel & ciRdNdx muxes in I2 stage
  by getting rid of tag index mux fanin on ciRdNdx.
ife/ife.V ife/ifpcselil.Veqn icc.V euterpe.V: Move iva/gva[47:15] pipe
  and snapped miss gva [47:12] to ICC so all in uniform place and to cut
  control back & forth.
ife/ife.V: Detect mispredict recovery to sequential new
  page & request corresponding hiccup to check protection.  Found by inspection;
  sinister protection implications if were not found.
lt/lt.V lt.control.pim euterpe.V icc.V rg/rGPC.V rg/rg.V pim:
  Delete ltlb xor data formerly sent to ICC so that it could do own xlation.
  Delete pc[63:48] sent to for ICC's version of ltlb translation.
  Replace 4 ranks of ff_16's with 2 ranks of hr_16 in base path.
at/atpaselgen8.Veqn (delete) at/atpaselgen8.V (add) at/Makefile:
  Reimplement so that gva input can be halfswing to handle new run to ICC.
at/at.V: Reorder dor pins into UfrcEnblR10 to be less X sensitive.
  Rearrange hardware ifetch access physical address forcing to not force
  gvaR8R9 input fullswing so can be halfswing to handle new run to ICC.
tst/spy.V: Eta spys were counting in wrong direction.
cj/Makefile: Add rsvdedepi.tst rule.
yy/tas.pl: Deposit/withdraw & copyswap had obsolete opcode-number assignments.
{ife,cj,tst}/*rst.tst tst/drvchk.V: update to match other recent changes.
ife/iffree.tst: Earlier new reset PC experiments had broken.
-----
revision 25.1
date: 1995/04/09 10:32:42; author: mws; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

```